PCB007 PRESENTS

March 2015

the pcb magazine

an I-Connect007 publication

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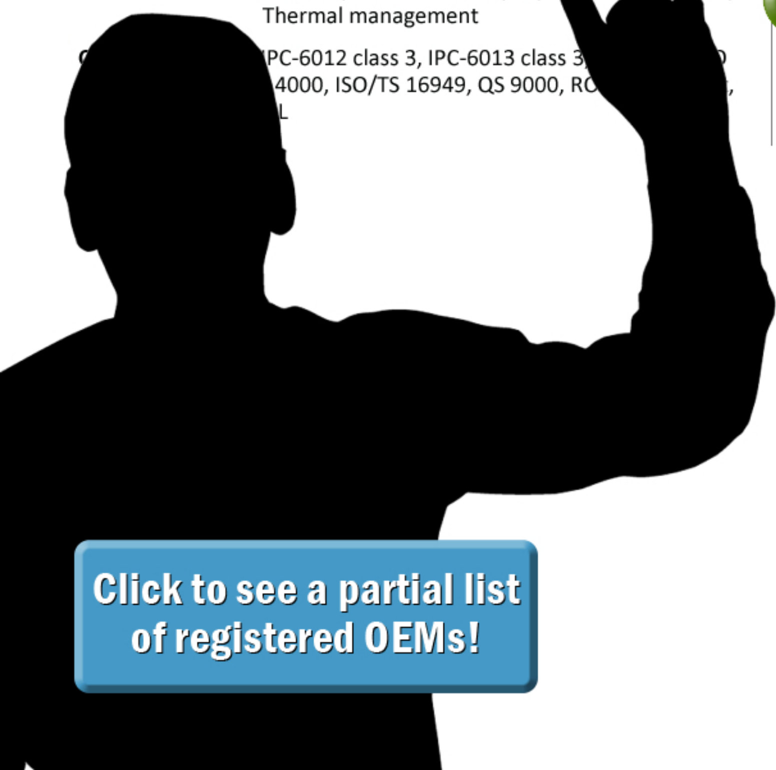

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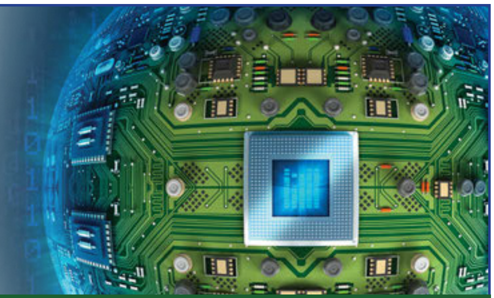

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*For more information, contact **Fern Abrams**, IPC director of regulatory affairs and government relations, at **FernAbrams@ipc.org***

March Featured Content

MATERIALS

This month, feature contributors from Isola, Ventec, OMG and Spirit Circuits examine the range of materials for multiple applications, including flame retardancy, high-speed designs, reliability testing and LED applications.

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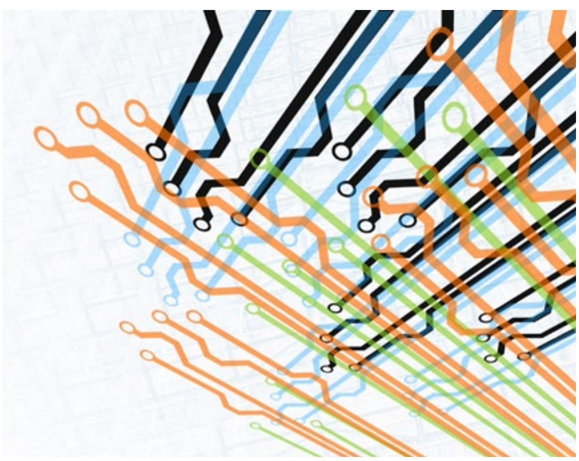
by Martin Cotton



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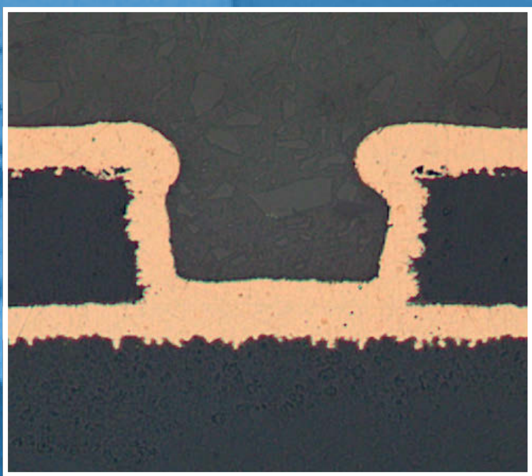
Electronics

Desmear and Metallization

Neoganth V8 Activator – New Economic Activator for Vertical MLB/HDI Manufacturing



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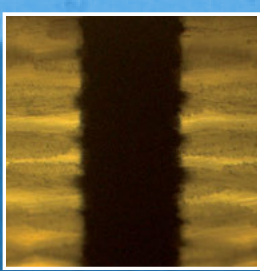
- Utilizable at low pH value resulting in less carbonate formation and therefore longer lifetime
- Excellent reliability performance
- Simple usage, no pH control necessary

Backlight Testing Results



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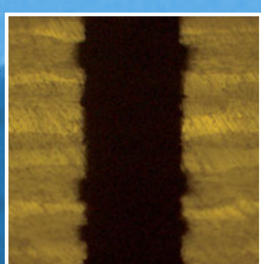

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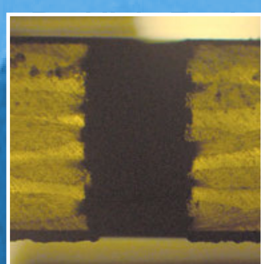
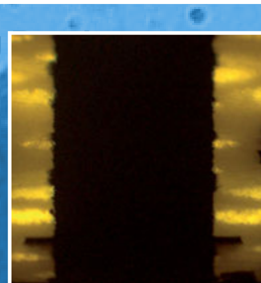


Isola DE104



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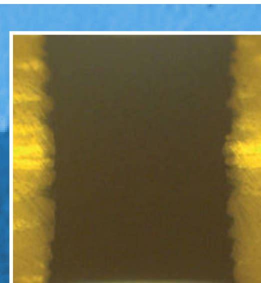

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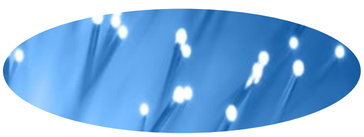

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FIRE RETARDANCY: WHAT, WHY, AND HOW

by Alun Morgan
EUROPEAN INSTITUTE OF PRINTED CIRCUITS

Abstract

This article takes a critical look at all aspects of fire retardancy, starting with the need for fire safety. The function of a flame retardant is examined and reactive and additive flame retardant classes are contrasted along with their chemical and physical effect mechanisms. Major flame retardant compounds, both halogen and halogen free, are examined in detail. Toxicology and Environmental impact are examined with particular emphasis on Tetrabromobisphenol-A which is the most widely used flame retardant in PCB materials. European legislative directives are also considered.

I. What are flame retardants?

Flame retardants are compounds, which when added to materials during or after manufacture, inhibit or suppress the combustion process.

They interfere with combustion at various stages of the process, e.g., during heating, decomposition, ignition or flame spread. Their primary function is to suppress the spread of fires or delay the time of flashover so that people can escape.

Flame retardants used in plastic materials fall broadly into two categories, namely additive and reactive. Additive flame retardants are incorporated and dispersed into the plastic prior to, during, or most commonly following polymerisation. If they are chemically compatible with the plastic they act as plasticisers oth-

erwise they are considered as fillers. Reactive flame retardants are chemically bound to the polymer molecule by incorporating them into the polymer backbone or by grafting them onto the backbone as branches. As reactive flame retardants are chemically bound to the host polymer they are prevented from bleeding out and thus generally exert greater flame retardancy than additive compounds due to their greater availability throughout the life cycle of the polymer into which they are incorporated.

"As reactive flame retardants are chemically bound to the host polymer they are prevented from bleeding out and thus generally exert greater flame retardancy than additive compounds due to their greater availability throughout the life cycle of the polymer into which they are incorporated."

II. Why do we need flame retardants?

On average there are more than 4,500 fatalities annually in the EU-27 as a result of fires; this accounts for 2% of all fatal injuries [1]. Fires develop from inception through build-up until a stage where the total thermal radiation from the fire-plume, hot gases and hot compartment boundaries cause the radiative ignition of all exposed combustible surfaces within the compartment. This sudden and sustained transition of a growing fire to a fully developed fire is called flashover [2]. At this point the radiation of energy to the contents of the room raises all the contents to their ignition temperature whereby the contents of the room suddenly and simultaneously ignite. It is estimated that in a domestic dwelling fitted with working fire alarms on all levels where the occupants are asleep upstairs and a fire starts on the main level of the residence the occupants have about three minutes to escape if they are to have any chance of survival[3]. The presence of flame retardants in otherwise combustible materials has two possible effects;

- The flame retardant may prevent the fire fom developing altogether or;
- The flame retardant may slow down the build-up phase of the fire thus delaying the onset of flash over thus extending the escape time window.

In either case, the flame retardant serves its primary purpose of reducing the risk of fire related fatalities.

The efficacy of the use of appropriate flame retardants can be seen by way of example from the introduction of "The Furniture and Furnishings Fire Safety Regulations" in the UK in 1988. These imposed a fire resistance requirement on all upholstered furniture supplied in the UK. Between 1988 and 2002 a Government commissioned report estimated that the "Furniture and Furnishings Fire Safety Regulations" played a direct role in saving 1,150 lives and preventing 13,442 injuries [4].

III. Flame Retardant Mechanisms

Flame retardants fulfil their purpose primarily by either physical or chemical action.

Physical action can be subdivided into three modes;

1. Cooling—An endothermic process is triggered by additives cooling the substrate to a temperature below that required for sustaining the combustion process.
2. Formation of protective layer—The combustible layer is shielded from the gaseous phase with a solid or gaseous protective layer. The oxygen required for the combustion process is excluded and heat transfer is impeded.
3. Dilution—Fillers are incorporated which evolve inert gases on decomposition diluting the fuel in the solid and gaseous phase so that the lower ignition limit of the gas mixture is not exceeded.

Chemical action can be subdivided into two modes:

1. Reaction in the solid phase—The flame retardant causes a layer of carbon to form on the polymer surface. This can occur through dehydration of the flame retardant forming a carbonaceous layer by cross-linking. The carbo-

naceous layer acts as an insulation layer, preventing further decomposition of the material.

2. Reaction in the gas phase—The free radical mechanism of the combustion process which takes place in the gas phase is interrupted. The exothermic processes are thus stopped, the system cools down and the supply of flammable gases is suppressed.

In printed circuit board material a number of these mechanisms are employed to achieve flame retardancy by appropriate choice of flame retardant compound. In some cases more than one mechanism is used and synergists can also be added to improve the efficacy of a primary flame retardant.

Halogenated flame retardants form the largest group of flame retardants used in printed circuit board materials.

Halogens comprise five chemically related highly reactive non-metallic elements found in group 17 of the periodic table. They are namely Fluorine, Chlorine, Bromine, Iodine and Astatine. The artificially created element 117 falls into group 17 and may also be classed as a halogen.

Since Astatine is amongst the rarest elements and occurs on Earth only as the result of the radioactive decay of heavier elements and element 117 is entirely synthetic with a half-life of less than one second these will not be considered further.

The other four Halogens, however, find many uses in everyday life (Table 1).

Fluorine and Iodine are not used as flame retardants as neither effectively interferes with the combustion process. Chlorine-containing flame retardants release HCl (hydrogen chloride) over a wide temperature range so the flame retardant concentration is reduced and is thus less effective.

Bromine is the most effective halogen flame retardant since its bonding to carbon enables it to interfere at a more favourable point in the combustion process. The effective agent, HBr (hydrogen bromide), is liberated over a narrow temperature range so that it is available at a high concentration in the flame zone.

The mechanism used by brominated flame retardants (BFRs), is that bromine breaks down to form a bromine radical which then reacts with the hydrocarbon to form HBr. The HBr removes the high energy H and OH radicals by reaction. The high energy radicals are replaced with low energy bromine radicals. The HBr consumed is then regenerated by reaction with the hydrocarbon (Figure 1).

In PCB substrates the bromine source is usually 2,2′,6,6′-Tetrabromo-4,4′-isopropylidenedi-

Fluorine	Chlorine	Bromine	Iodine
- UF_6 Used for Uranium Enrichment - Fluoroplastics PTFE (Teflon) Viton (synthetic rubber) - SF_6 Gaseous insulator in high voltage switchgear - NaF, SnF_2, Na_2PO_3F Anti decay additive in toothpaste	- NaCl, Table salt - PVC Pipes, building materials, electrical insulation, clothing - $SiCl_4$ Manufacture of Silicon for semiconductors - HCl - Medicine - Pesticide - Indispensable to life	- Flame retardants - Biocides - Water treatment - Pharmaceuticals - Crop protection - Mercury abatement - Clear Brine Fluids for drilling. - Naturally occurring in mandarins.	- Thyroid hormone production - Dietary supplement - X-ray contrast agent - Chemical catalyst, for example in epoxy resin manufacture - Water purification - Antiseptic - Halogen lighting - Indispensible to life

Table 1.

phenol (Tetrabromobisphenol-A or TBBPA) and this is incorporated as an additive flame.

In the category of non-halogenated flame retardants phosphorous containing compounds are the most popular and of these 9,10-Dihydro-9-Oxa-10-Phosphaphenantrene-10-Oxide (DOPO) is the most widely used. The compound is reacted as an additive flame retardant. The flame retardant mechanism is that the phosphorus containing compound is converted by thermal decomposition to phosphoric acid. The phosphoric acid then dehydrates the oxygen containing polymer and causes charring (Figure 2).

The metal hydroxide alumina trihydrate (ATH, gibbsite) is a widely used synergist in non-halogen flame retardant systems.

The flame retardant mechanism of ATH is physical and combines cooling with the formation of a protective layer and gaseous phase dilution. The ATH breaks down around 200ºC to aluminium oxide in an endothermic reaction with the release of water vapour. The resulting endotherm cools the polymer so fewer pyrolysis products are formed. The aluminium oxide, together with the charring products formed on the substrate acts as an insulating protective layer and the water vapour liberated has a diluting effect in the gas phase and forms an oxygen displacing protective layer.

It is reported that undesired release of water due to thermal decomposition in multiple soldering operations in ATH systems may lead to a loss of the effectiveness of flame retardancy, reduced CAF (conductive anodic filamentation) performance and delamination. Aluminium monohydrate (AlOOH, boehmite) has been proposed as a thermally stable alternative [5].

IV. Halogen-Free?

In the context of printed circuit board materials halogen-free can be broadly interpreted

⇨ The bromine breaks down to form a bromine radical which then reacts with the hydrocarbon to form HBr.

$$\mathrm{R{-}Br} \longrightarrow \mathrm{R\bullet} + \mathrm{Br\bullet}$$

$$\mathrm{R{-}H} + \mathrm{Br\bullet} \longrightarrow \mathrm{R\bullet} + \mathrm{HBr}$$

⇨ The HBr removes the high energy H and OH radicals by reaction.
The high energy radicals are replaced with low energy bromine radicals.

$$\mathrm{HBr} + \mathrm{OH\bullet} \longrightarrow \mathrm{H_2O} + \mathrm{Br\bullet}$$

$$\mathrm{HBr} + \mathrm{H\bullet} \longrightarrow \mathrm{H_2} + \mathrm{Br\bullet}$$

⇨ The HBr consumed is regenerated by reaction with the hydrocarbon.

$$\mathrm{R{-}H} + \mathrm{Br\bullet} \longrightarrow \mathrm{R\bullet} + \mathrm{HBr}$$

Figure 1.

as "free of halogenated flame retardant." Indeed the IEC defines halogen free thus[6]:

- 900 ppm maximum chlorine
- 900 ppm maximum bromine
- 1500 ppm maximum total halogens

It is necessary to have such a definition as halogens are always present to some extent. Epoxy resins, for example, are produced by reacting bisphenol-A with epichlorohydrin, which contains chlorine. Therefore all epoxy resins contain measurable traces of chlorine; iodine is also widely used as a necessary constituent of the catalyst used in epoxy resin production.

It is an interesting diversion to consider PTFE materials which are used in some PCB applications. PTFE contains fluorine which is highly toxic and the most reactive halogen but seems to have largely escaped attention in the context of halogen free materials. However, in PTFE the fluorine is tightly bound to the carbon atoms and is therefore not available as free fluorine. It is useful here to underline the distinction between compounds and native elements and their respective physical and chemical properties. The best common example would be that of table salt, NaCl which comprises the elements sodium and chlorine. Sodium is a highly reactive metal and is classified as being very hazardous in case of skin contact and chlorine is a highly corrosive toxic gas. However, the two elements combine to form sodium chloride which is benign and essential to human life.

The same distinction must be drawn when considering flame retardants incorporating phosphorous and bromine. These are toxic in elemental form; however when used reactively as flame retardants have limited bioavailability and as such do not pose any significant threats to human life or the environment.

V. Toxicology Studies

There have been many studies into the toxicology of flame retardants and there is no sign of activity in this area abating. It is of great importance that people are protected from risk of death or serious injury by fire, but also that the systems used to provide that protection do so without adding risks to human health or the environment. The most widely used flame retardant in PCB materials is Tetrabromobisphenol-A or TBBPA, and is amongst the most studied flame retardants.

A study carried out in 1999 by the University of Surrey[7] assessed the risks posed by com-

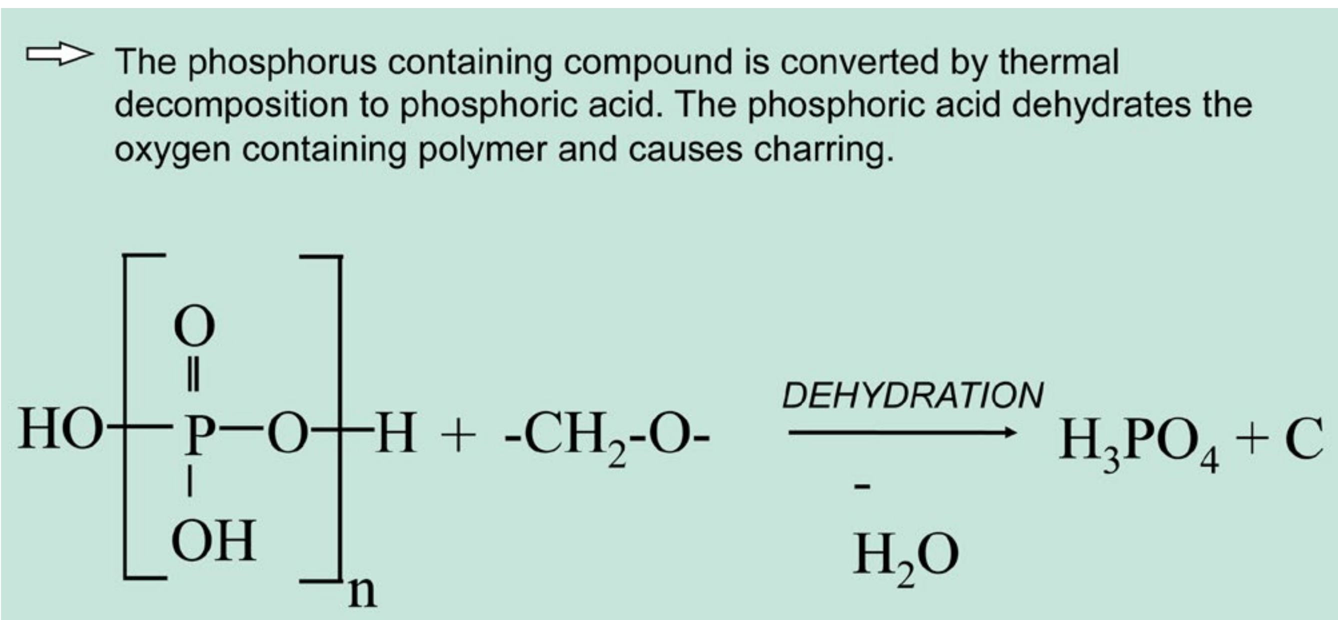

Figure 2.

- Aluminium Trihydrate (ATH) breaks down around 200°C to Aluminium oxide in an endothermic reaction with the release of water vapour.

$$2\,Al(OH)_3 \xrightarrow[-298\ \text{kJ/mole}]{\Delta} Al_2O_3 + 3H_2O$$

- As a result of the endotherm the polymer is cooled therefore fewer pyrolysis products are formed
- The Aluminium Oxide, together with the charring products formed on the substrate acts as an insulating protective layer
- The water vapour liberated has a diluting effect in the gas phase and forms an oxygen displacing protective layer.

Figure 3.

mon flame retardants, including TBBPA and concluded for the smoke and gases released in case of fire: "The major hazards of most fires arise from the existence of the fire and not the materials burned and there is no evidence that flame retardants contribute to the direct human health risks arising from toxic gas effects."

The report also concluded: "Examination of the toxicology of six of the more common flame retardants used in consumer products indicates that in general they do not pose any significant threats to human life and the environment. Moreover any indication of risk from the toxicology of flame retardants themselves in isolation will be exaggerated because of their limited bioavailability when they are incorporated into a polymer matrix."

Under the framework of the European risk assessment (RA) a report into the human health risks of exposure to TBBPA published in 2006 concluded[7]:

Human health: No health effects of concern have been identified for TBBPA.

Workers

Conclusion (ii) There is at present no need for further information and/or testing and no need for risk reduction measures beyond those which are being applied already.

No health effects of concern to adults have been identified. Therefore conclusion (ii) is reached in relation to all endpoints and for all exposure scenarios.

Consumer:

Conclusion (ii) There is at present no need for further information and/or testing and for risk reduction measures beyond those which are being applied already.

Given that consumer exposure is negligible conclusion (ii) is reached in relation to all endpoints.

Underlining the use of TBBPA as an additive flame retardant, BSEF states[8]:

TBBPA is classified in the EU as an H410 substance, which means that it is toxic to aquatic

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organisms and it has to be labeled to reflect this classification. However, TBBPA loses this classification when it is reacted into the printed circuit board resin, which represents more than 80% of its uses. TBBPA is employed as a starting material that fully reacts to form the epoxy resins of laminates for printed circuit boards. This full integration into the epoxy resin ensures that the final product, flame retarded printed circuit boards, no longer contains TBBPA, leaving the user free from any possible exposure.

VI. REACH and RoHS

REACH is a European Union regulation concerning the registration, evaluation, authorisation and restriction of chemicals. It came into force on 1st June 2007 and replaced a number of European Directives and Regulations with a single system. The aim of REACH is to improve the protection of human health and the environment through early identification of hazardous properties in chemical substances while maintaining the competitiveness and enhancing the innovative capability of the EU chemicals industry. REACH requires registration of substances manufactured or imported into the EU in quantities of 1 tonne or more per year. TBBPA was registered under REACH in October 2010.

Under the REACH regulations, substances that may have serious and often irreversible effects on human health and the environment can be identified as substances of very high concern (SVHCs). If a substance is identified as an SVHC, it will be added to the Candidate List for eventual inclusion in the Authorisation List. As at 13 December 2013 the candidate list of SVHCs numbered 151 substances[9]. TBBPA is not included as a SVHC.

The Restriction of Hazardous Substances Directive 2002/95/EC (RoHS), was adopted in the European Union in February 2003 and restricts the use of six hazardous materials in the manufacture of various types of electronic and electrical equipment. Polybrominated biphenyls (PBB) and Polybrominated diphenyl ether were among the restricted materials. No restrictions were placed on the use or manufacture of TBBPA.

RoHS was revised in 2011 (RoHS II): no new substance restrictions were added, but provision was made for future substance review by the Commission.

Currently the Commission is working on developing the methodology for future substance restrictions. The final methodology will be published in July 2014.

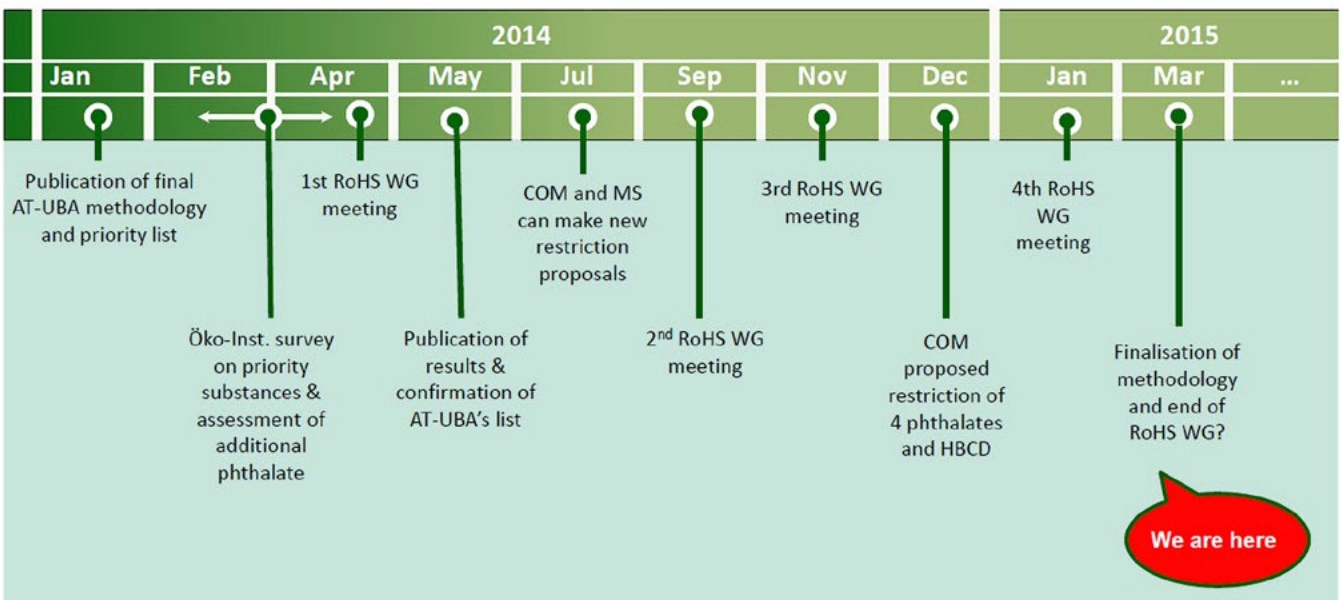

Figure 4: The timeline of RoHS II[10].

The Austrian Environment Agency on behalf of the Commission developed the first draft of the methodology and identified substances used in E&E for future evaluations. The Commission is now organising a working group of stakeholders to finalise the last stage of the methodology. Each substance will be evaluated on an individual basis, taking into account all existing science. Both Member States and the Commission can nominate substances

TBBPA has been identified as a substance for future reviews under the RoHS as it is used in electronic and electrical equipment.

VII. Flame Retardants and the Future

Neils Bohr famously said *"Prediction is very difficult, especially if it's about the future."* Fire safety will surely remain a primary requirement for electronic and electrical equipment. In order to ensure fire safety there will be a need to incorporate flame retardants to plastic systems forming part of such electronic and electrical equipment that would otherwise pose a significant fire safety risk.

Halogenated materials form by far the largest group of flame retardants used in PCB materials with a global estimated market share of greater than 80%. In Europe the figure is estimated to be nearer to 95%.

UL have recognized that traditional FR-4[11] materials have evolved in recent years and now represent a diverse family of materials. In recognising this, for testing purposes UL have now divided the FR-4 category into two sub-categories, FR-4.0 and FR-4.1[12] (Figure 5).

The new UL classifications of FR-4.0 and FR-4.1 divide the materials into brominated and non-halogen, respectively.

There is no clear scientific evidence based driver to restrict the use of halogenated flame retardants. Legislation under REACH and RoHS II should be expected to apply rigorous scientific methodology in assessing risks to human health; such studies to date have not raised concerns about the continued use of halogenated flame retardants.

Performance requirements are driving PCB materials suppliers to develop materials for high-speed applications whilst improving electrical and thermal reliability. However, ultimately consumer choice is also a driver and may well play into the market vector of high speed and high reliability requirements. **PCB**

References

1. EuroSafe, Injuries in the European Union, Report on injury statistics 2008-2010, Amsterdam, 2013

New UL/ANSI Types Replacing FR-4 from IPC proposal

UL/ANSI Type	Primary Resin	Secondary Resin(s)	Filler[1]	Flame Retardant	Reinforcement
FR-4.0 (Brominated FR-4)	Epoxy[2]	Any	Inorganic Max 45%	Bromine	Woven Glass
FR-4.1 (Non-Halogen FR-4)	Epoxy[2]	Any	Inorganic Max 45%	Non-Halogen	Woven Glass

[1] Examples of inorganic fillers include, but are not limited to: Silica, Clay, Talc, Ceramic, Calcium Carbonate, Aluminum Hydroxide, Fumed Silica and Titanium Oxide.

[2] Epoxy functionality, minimum 50% by weight of organic resin.

Figure 5.

2. Fire Research Station, UK 1993.
3. Fire Engineering®. Glenn A. Gaines, Deputy U.S. Fire Administrator.
4. Paul Farley in *Furniture News,* Jan 29, 2014.
5. Dr. Oliver Töpfer, Nabaltec. "Boehmite as Halogen Free Flame Retardant Filler Utilized in Cost Effective Producton of Highly Reliable Base Laminates," EIPC Summer Conference, Milan, September 2012.
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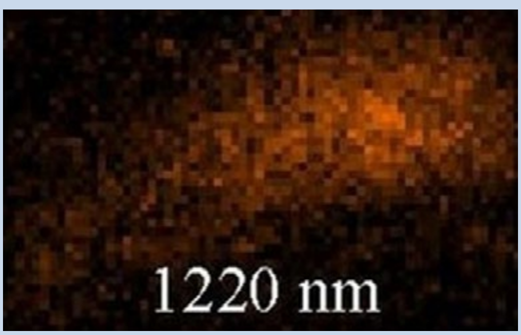
Alun Morgan is chairman of the European Institute of Printed Circuits.

Predicting Metamaterial Nonlinear Optical Properties

Metamaterials—artificial nanostructures engineered with electromagnetic properties not found in nature—offer tantalizing future prospects such as high resolution optical microscopes and superfast optical computers. To realize the vast potential of metamaterials, however, scientists will need to hone their understanding of the fundamental physics behind them. This will require accurately predicting nonlinear optical properties—meaning that interaction with light changes a material's properties, for example, light emerges from the material with a different frequency than when it entered. Help has arrived.

Scientists with the U.S. Department of Energy (DOE)'s Lawrence Berkeley National Laboratory (Berkeley Lab) and the University of California (UC) Berkeley have shown, using a recent theory for nonlinear light scattering when light passes through nanostructures, that it is possible to predict the nonlinear optical properties of metamaterials.



"The key question has been whether one can determine the nonlinear behavior of metamaterials from their exotic linear behavior," says Xiang Zhang, director of Berkeley Lab's Materials Sciences Division and an international authority on metamaterial engineering who led this study. "We've shown that the relative nonlinear susceptibility of large classes of metamaterials can be predicted using a comprehensive nonlinear scattering theory. This will allow us to efficiently design metamaterials with strong nonlinearity for important applications such as coherent Raman sensing, entangled photon generation and frequency conversion."

Zhang, who holds the Ernest S. Kuh Endowed Chair at UC Berkeley and is a member of the Kavli Energy NanoSciences Institute at Berkeley (Kavli ENSI), is the corresponding author of a paper describing this research in the journal Nature Materials. The paper is titled "Predicting nonlinear properties of metamaterials from the linear response." The other authors are Kevin O'Brien, Haim Suchowski, Junsuk Rho, Alessandro Salandrino, Boubacar Kante and Xiaobo Yin.

FEATURE

Make the Right Decisions at the Right Time in the PCB Design Process

by Martin Cotton
VENTEC INTERNATIONAL GROUP

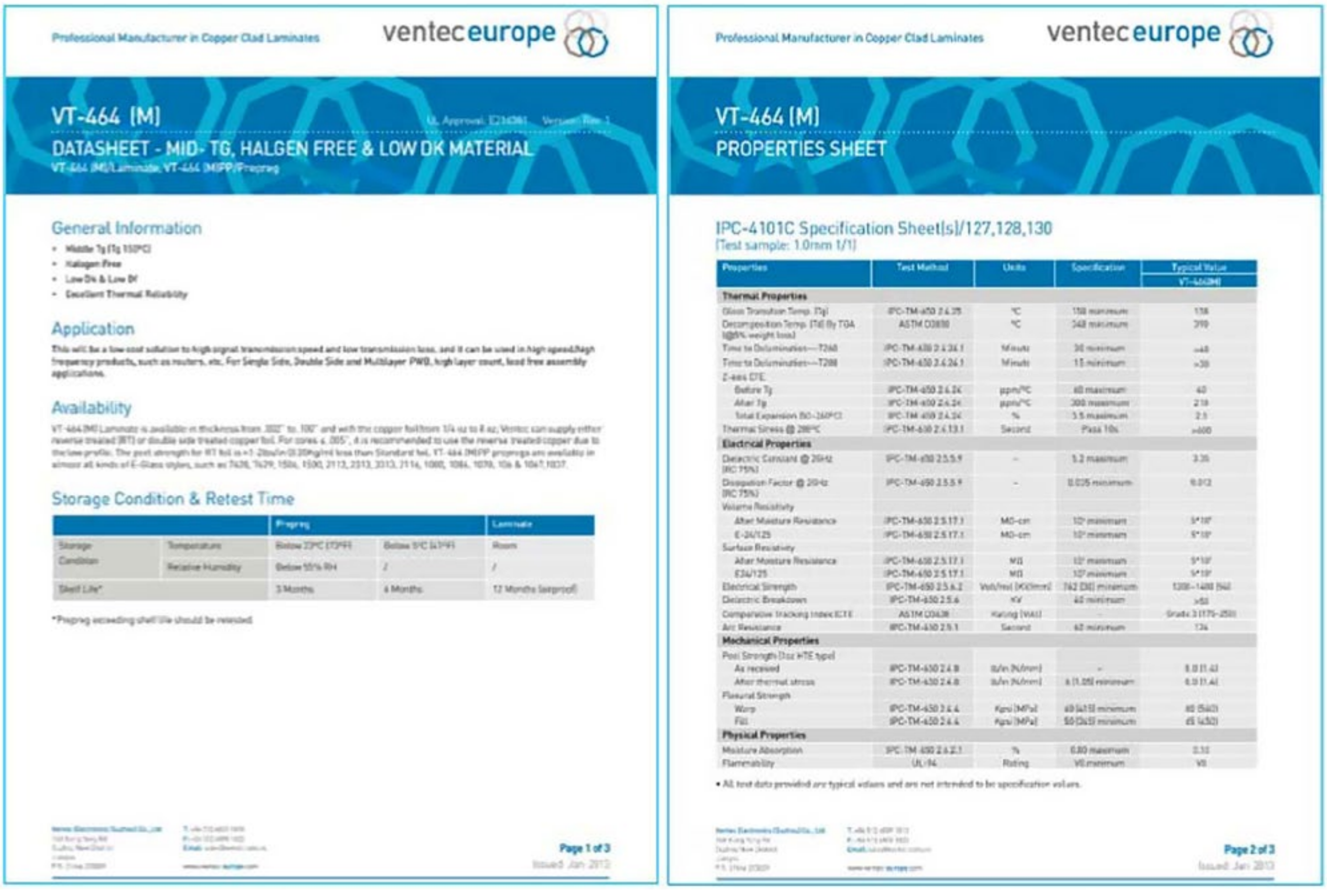
The right decisions are not always the easiest decisions, but making them well and as early as possible often avoids errors and addition costs. This is certainly the case in PCB design and a key decision influencing the design process and the eventual outcome is the selection of material and of the materials vendor. This is even more important when the PCB requires significant performance parameters to be met, such as high speeds.

What I am not trying to do is teach hardware or PCB design. What I am seeking to do is to consider the processes that lead to successful design and the errors that lead to risk, potential problems and compromises.

Let's take an example of a back plane design that has been specified at 10Gbs with 100ohm impedance with a design target of 36 layers.

First, we need to ensure that we fully understand what the specification means. Are we sure we mean 10Gbs, which is a data rate in gigabits per second, and not 10Ghz, which is a frequency? Are we seeking that data rate for a single channel, or do we need that rate for a buss? The buss speed is the total of all the channels in that buss.

The next task would be to consider the design rules we'd like to apply based on the need for 100 ohms of differential impedance using two tracks that are in harmony so that losses


Professional Manufacturer in Copper Clad Laminates

ventec europe

VT-464 (M)

DATASHEET - MID- TG, HALGEN FREE & LOW DK MATERIAL

General Information

Application

Availability

Storage Condition & Retest Time

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ventec europe

VT-464 (M)

PROPERTIES SHEET

IPC-4101C Specification Sheet(s)/127,128,130

(Test sample: 1.0mm 1/1)

Thermal Properties

Electrical Properties

Mechanical Properties

Physical Properties

Page 2 of 3

Figure 1: Typical supplier specification.

are minimized. The geometry of those tracks and their positioning with the PCB structure are critical to realizing a good design that can be manufactured with a good yield.

The design is only good when the specifications are met and the PCB can be manufactured with a good yield.

Now is the time to consider materials, because setting up differential pairs in the X, Y & Z axis requires we know and understand the Dk (dielectric constant) and Df (dissipation factor) of the material. Materials specifications are a good starting point. After all the suppliers will have designed the material with a purpose, so they will have a particular data rate in mind. But not all material suppliers are the same. Some will have design experience and some will not. Some are distributors, whilst others will have direct access to the staff at the laminator who designed the materials to meet a particular need in the market. Choose the vendor carefully and work closely with them to get the right material designed in, and agree design rules appropriate to that material and to your needs. They'll need to have experience of the fabrication process as well as design and be able to support you in working with the PCB manufacturer throughout the prototype and volume manufacturing process.

You're now ready to create the specification of the 'cells'—the traces, trace separation, pair separation, and the layer-to-layer separation. Again, the materials team should be able to support this and you should certainly be sharing it with them before starting the design. Impedance modeling can be performed at this stage using modeling software, such as that offered by Polar Instruments and other companies. The material Dk will have a substantial effect at this point impacting upon layer separation

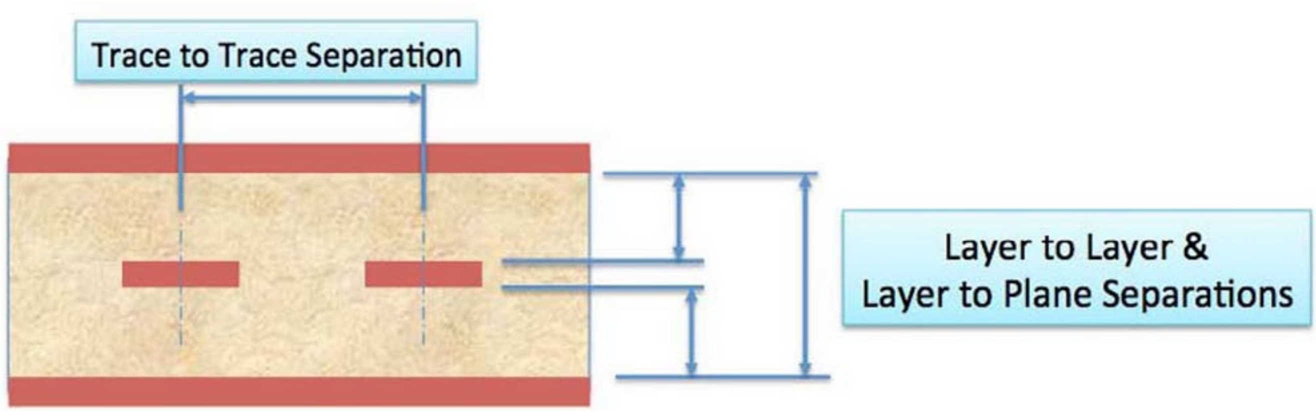

Figure 2: The completed cell.

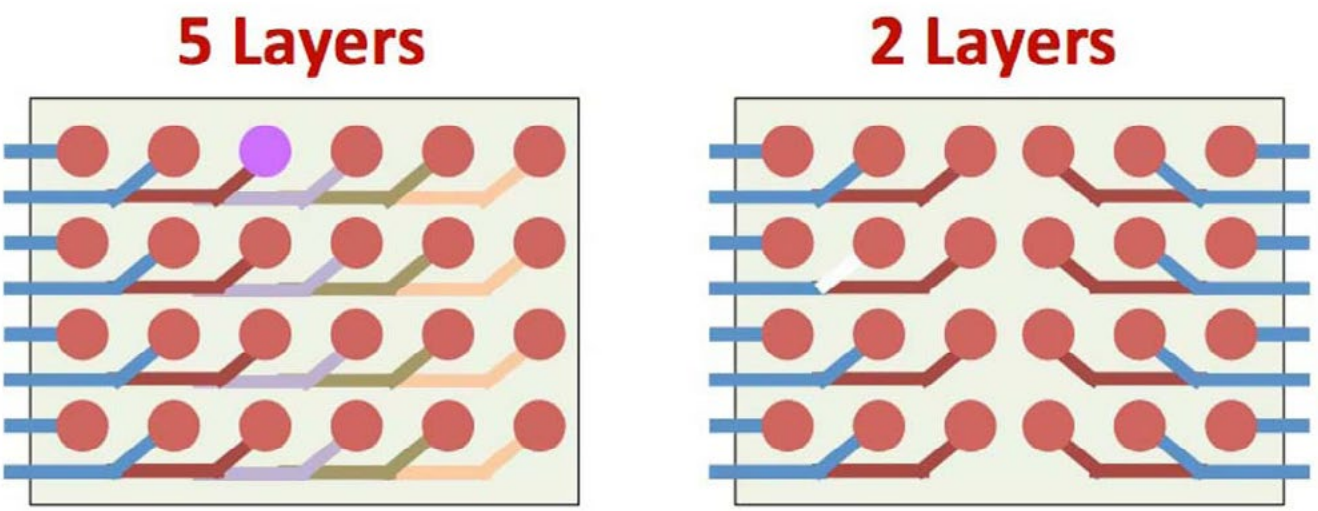

Figure 3: Trace mapping and depth of complexity (DoC).

and trace width. Df considerations are also critical in designing a successful cell that has the appropriate trace, pair and layer separation. It is worth spending time at this stage to get the right cell design and the right material, as it will impact everything moving forward.

With the cell as the heart of the design and the right material selected the stack up can be created, again with the support of the laminate manufacturer and the PCB fabricator. Key to understanding the impact of density on layer count and stack up is mapping the densest devices on the PCB, such as BGAs and connectors. Depth of Complexity (DoC) is a methodology for measuring and calculating initial layer requirements. Mapping power distribution and layers is essential at this stage in establishing how many layers are required to realize a successful design. And remember by successful we mean within specification and with a high level of manufacturability.

Having created the cell structure, the design rule, the orthogonal design and having selected the material and build we can estimate the cost and start the design. Again a good time to make sure everything is synchronized with the laminate supplier and the fabricator. Throughout layout additional checks and simulations are made to ensure we are meeting our specifications for good signal integrity (SI).

Having done it right so far, this is no time to lose your nerve.

The first pass of the design layout may not produce the perfect result. Let's imagine the post layout simulation reveals we have SI issues with 90 differential pairs of the 2,000 that we have used. This leaves us two choices. The hard way—fix them by individual review or the easy way—add four more layers dedicated to the 90 pairs. Clearly the hard way is the better way, but that takes time and that time requires skills, not just machines. This is where good designers stand out and can really earn their money. All too often the easy way is chosen, more layers are added, a materials upgrade is chosen with better performance and higher costs, often in the order of 15–25% are added.

In the case of our example, the hard way resulted in a board meeting the 36-layer target that fits mechanically and is easily manufacturable at the target cost of $1,200. The easy way delivered a 42-layer board, with less readily available materials, which is harder to manufacture, costs $1,550 and impacts on other parts of the mechanical design, due to having impacted on board thickness.

The right way is undoubtedly the harder way, and the results will be savings enjoyed throughout the life of the product, greater reliability, more manufacturing flexibility and a real sense of satisfaction in getting it right.

Choosing a laminate is important, choosing a laminate supplier is even more important. A supplier or distributor can provide you with what you ask for, but a laminate partner will provide you with design and fabrication support throughout, helping you get it right first time. **PCB**


Martin Cotton is director of OEM technology for Ventec International Group.

FEATURE

Reliability Testing and Statistics

by Patrick Valentine
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What is reliability? Reliability is the probability of a product performing its intended function over its specified period of usage, and under specified operating conditions, in a manner that meets or exceeds customer expectations[1].

The catalyst for the emergence of reliability analysis goes back to 1906, when Lee de Forest invented the triode vacuum tube. The vacuum tube initiated the electronics revolution, enabling a series of applications such as the radio, television, radar, etc. The vacuum tube is recognized by many as the technology that allowed the Allies to win the so-called "Wizard War" of World War II. Ironically the vacuum tube was the main cause of equipment failure and tube replacements were needed five times more often than all other equipment[2].

In 1937, Waloddi Weibull invented the Weibull distribution, and in 1951 he delivered his hallmark American paper on this subject claiming that his distribution applied to a wide range of problems. He showed several examples ranging from fiber strength of cotton to the fatigue life of steel[3]. In 1952 the Advisory Group on Reliability of Electronic Equipment (AGREE) was jointly established by the Department of Defense (DoD) and the American Electronics Industry. In 1956 the Radio Corporation of America (RCA), a major manufacturer of vacuum tubes, released a significant report, "Reliability Stress Analysis for Electronic Equipment" (TR-1100), which presented a number of models for estimating failure rates. Then, in 1959, the "RADC Reliability Notebook" came into existence, and in 1961, a military reliability prediction handbook format known as MIL-HDBK-217 was published. Numerous other reliability documents have been published ever since.

Historically, reliability engineering of electronics has been dominated by the belief that the life or percentage of complex hardware failures that occur over time can be estimated, predicted, or modeled. Ironically, there is little, if any, empirical field data from the vast majority of verified failures that shows any correlation with calculated predictions of failure rates[4].

Modern reliability tests try and simulate assembly and field use conditions. These methods include solder shock, air-to-air thermal cycling, liquid-to-liquid thermal cycling, interconnect

stress test (IST), and highly accelerated thermal stress (HATS, an air-to-air method). Reliability test conditions can and do vary widely by OEMs. We see resistive heating pre-conditioning cycles at 260°C for six times, followed by resistive heating thermal cycling at 190°C, current induced thermal cycle of -23°C to +220°C, and air-to-air cycles of -60°C to +160°C[5]. Why such harsh testing conditions? What are we trying to prove? And can it be proved? At this rate, testing conditions are destined to become even more severe with the acceptance criteria shrinking to very tight tolerances. Often in reliability testing, the threshold value for determining failure is chosen subjectively[6].

Current industry views on reliability consist of customer requirements and results based on a variety of reliability testing procedures. However, there is still no consensus within the industry as to what each of the reliability test protocols prove and when each test protocol has to be used[5]. The challenge in reliability testing is correlating testing conditions to field use[6, 7, 11].

At the heart of the printed circuit board we find interconnects, plated through holes (PTH), and microvias. These features must be robust for today's demanding mission critical applications. The shift to lead-free soldering has had the largest impact on electronic assembly reliability, both printed circuit boards as well as components. Assembly and rework are the most critical operations that can consume a significant amount PTH's useful life. And the plated through-hole represents one of the most significant failure modes from a reliability perspective, with many conditions in the design of the product influencing the reliability of the plated through hole structure[5].

Reliability testing can also be used in the research lab to validate new products and processes. Using designed experiments and reliability analysis, one can validate that a new product or process is as reliable as, or more reliable than, the current product or process[6].

"Reliability testing can also be used in the research lab to validate new products and processes. Using designed experiments and reliability analysis, one can validate that a new product or process is as reliable as, or more reliable than, the current product or process."

How severe should reliability testing be to simulate assembly and field use conditions?

Before we get into that, a review of basic reliability terms is in order. Let's define several terms in alphabetical order:

Anderson-Darling Statistic: Relative goodness-of-fit measure for the selected distribution. One can compare the AD statistic for several different distributions with the same number of parameters; smaller AD values indicate that the fit is better. Note: the AD statistic is not restricted to reliability applications.

Bathtub Curve: A conceptual model for describing reliability-related phenomena at the component level over its life cycle. Consists of three stages: infant mortality, design life, and wearout.

Beta (β): Determines the shape of the Weibull distribution. Referred to as the "shape" parameter.

Censoring: when exact failure times are not known (the test was stopped before a failure occurred). We call this "right" censored data. Usually "0" is used for censoring and "1" is used for actual failures.

Competing Failure Modes: when there are two or more failure modes present. It is best practice to analyze multiple failure modes separately when failure modes behave differently.

Confidence Intervals: a range of values, derived from sample data, which is likely to contain the value of an unknown population parameter. A 95% interval means 19 out of 20 samples (95%) from the same population will produce confidence intervals that contain the population parameter. In reliability, we gener-

ally use 95% and are interested in the lower bound as a worst case scenario.

Correlation Coefficient (Pearson's): measures the strength of the linear relationship between the data set and the chosen distribution. If the distribution fits the data well, when the points are plotted on a probability plot graph, these points will fall on a straight line (superimposed on, or very close to, the diagonal line) and the correlation coefficient will approach 1. Carries a maximum value of 1.

Distributions: a spatial array of data values, or the space in which the data occupy. An empirical distribution is based on sample data, whereas a theoretical distribution is based on possible values of a random variable. Weibull and Lognormal are the most frequently used distributions.

Estimation Methods: least squares or maximum likelihood methods.

Equality of Parameters: statistical test to check whether two or more data sets have the same shape, scale, or threshold parameter. Typical tests return a 95% confidence interval and a p-value; the default p-value for statistical significance is 0.05 ($\alpha = 0.05$), so a p-value below this is statistically significant (there is a statistical difference).

Eta (η): determines the spread of the Weibull distribution. A larger Eta value stretches the distribution, while a smaller Eta value squeezes the distribution. For the Weibull distribution it's always the 63.21 percentile of the distribution. Referred to as the "scale" parameter.

Hazard Function: a measure of the likelihood of failure as a function of time, and is unique for each distribution.

Infant Mortality ($\beta < 1$): failures that occur early during reliability testing and are caused by manufacturing defects such as poor workmanship, out-of-spec processing, substandard manufacturing and/or assembly practices, etc.

Lower / Upper Bound: Confidence intervals are often not symmetric about the estimate, so we specify precision as a distance to the estimated lower or upper bound. We generally use the lower bound as a worst case scenario when a large parameter value is considered good. Conversely, if the proportion of nonconforming units was being estimated, the upper confidence limit would be the worst case scenario.

Lognormal: the second most commonly used distribution in reliability to explain the location [Mean (μ)] and scale [Std Dev (σ)] of the data. This distribution has a lower bound (left tail) that is zero (0). The threshold parameter can be set to any positive value to move the lower bound.

MTTF (mean time to failure): a measure of the center of the distribution of failure times, the average or expected failure time that takes into account censored observations.

Nonparametric: does not use, or make assumptions about the parameters of a population.

Parameters: unknown population values that are estimated by the values of corresponding sample statistics. The lognormal distribution has two parameters, location, and scale, with a third optional nonzero threshold parameter. Likewise, the Weibull distribution has two parameters: shape and scale, with a third optional nonzero threshold parameter.

Parametric: a distribution described by one or more parameters. For example, the normal distribution family is identified by its mean (μ) and standard deviation (σ).

Percent: percent of population that has failed.

Percentile: time of failure (e.g., days, hours, cycles, etc.).

Precision: the distance from the estimate to either the lower or upper bound of the corresponding confidence interval.

R by C Notation: signifies what reliability requirement (R) at time (t) we want to meet with level of confidence (C). A R95C95 means 95% probability of survival, R(t), with 95% confidence in achieving that requirement. R(t) is viewed as a lower confidence limit on reliability, denoted as R_L.

Reliability: percentage of units that will survive a certain length of time.

R-Squared (r^2): the coefficient of determination that represents the proportion of variation that is explained. Calculated by squaring the correlation coefficient. Maximum value of 1.

Threshold: parameter that provides an estimate of the earliest failure time.

Useful Life (β = 1): a constant failure rate (constant % fails in the next unit of time) with random failures (independent of time) due to excessively high loads, environmentally induced stresses, etc.

Wearout, Early (1 < β < 4): early wearout begins with failures of weaker items and progresses to wearout of stronger parts as β moves from 1 to 4. Failures occur due to low cycle fatigue, corrosion, aging, friction, etc.

Wearout, Rapid (β > 4): highly reliably products, failures occur due to fatigue, corrosion, aging, friction, etc.

Weibayes: a method that combines the Weibull distribution with Bayesian statistics to analyze reliability data that have no failures. To use this method, there are four criteria that must be met.

Weibull: the most commonly used distribution in reliability used to explain the shape [Beta (β)] and scale [Eta (η)] of the data. This distribution has a lower bound (left tail) that is zero (0). The threshold parameter can be set to any positive value to move the lower bound.

Now that we have an understanding of the basic terms used in reliability, let's take a closer look at the bathtub curve and its meaning. Figure 1 shows the bathtub curve with its three stages.

The three stages of the bathtub curve are described in table 1.

Of importance is the interpretation of the shape (β) in reference to the scale (η). Steep (large) shapes (β) within the design life are a source of concern as there is risk of the entire population failing quickly as the parts age into the steep Weibull shape. On the other hand, if the Weibull scale (η) is well beyond the design life, there is negligible probability of failure before part retirement. In this case, steep shapes (β) are a source of happiness. Most steep shapes (β) have a safe period before the onset of failures, where the prob-

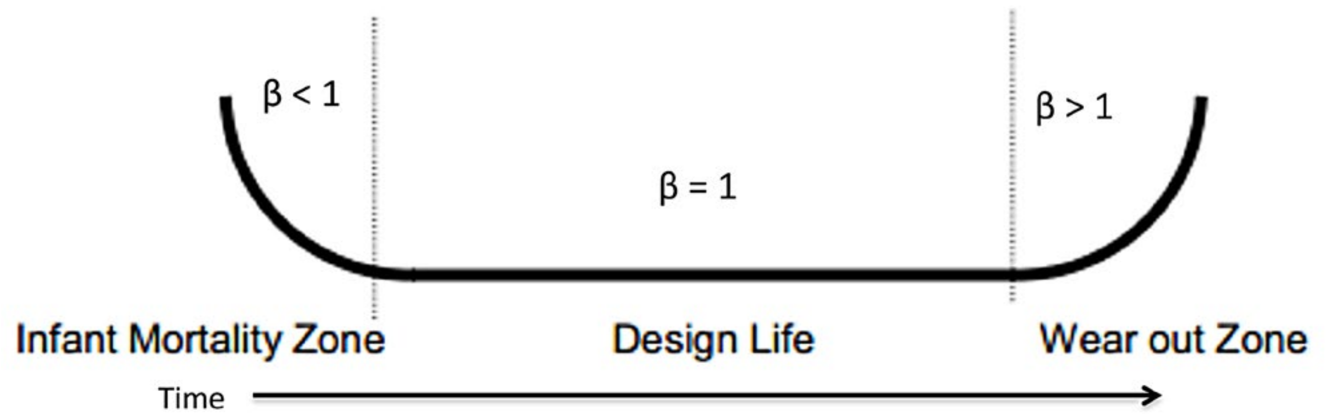

Figure 1: Bathtub curve with its three stages.

Stage	Beta (β)	Characterized by	Caused by
Infant Mortality	< 1	Decreasing hazard (failure) rate as time goes on	Manufacturing defects Out-of-spec processing Quality control problems
Design Life	= 1	Constant hazard (failure) rate as time goes on[1]	Environmentally induced stresses Excessively high loads Maintenance errors, human errors
Wearout	> 1	Increasing hazard (failure) rate as time goes on	Fatigue Corrosion Friction

[1]Constant % fails in the next unit of time, with random failures (independent of time)

Table 1: The three stages of the bathtub curve.

ability of failure is negligible. The steeper the shape (β), the smaller the variation in times to failure and the more predictable the results of the product. A vertical shape (β) of infinity implies perfect design, manufacturing, and quality control[8].

For example, let's say we have a product that is required to pass 100 thermal cycles. We run two lots and get the following results:

	Lot 1	**Lot 2**
Shape (β)	3.4	3.9
Scale (η)	250	125

Lot 2 has a steeper (larger) shape (β) value and we might interpret this lot as more reliable, but when we consider the scale (η), value lot 1 has 2x that of lot 2. In other words, lot 1 performance is well beyond the design life (100 cycles) and the probability of failure occurring within the design life is negligible.

Here's another worked example: Table 2 has plated through-hole thermal cycling data. The data is censored at 300 cycles and is coded as such with 1 = failure, 0 = right censored.

Using software, we can fit a distribution to the data set[9]. The first look at the Weibull plot answers two questions: How good is the fit and what is the beta (β), the slope? (Figure 2)

Cycles	Censor
200	1
160	1
222	1
175	1
250	1
300	0

Table 2: PTH thermal cycling data.

The correlation coefficient is 0.976, and the data points line up well on the diagonal line indicating we have a good fit. The origin of the blue diagonal line comes from the shape (β) and scale (η) parameters iteratively derived from the

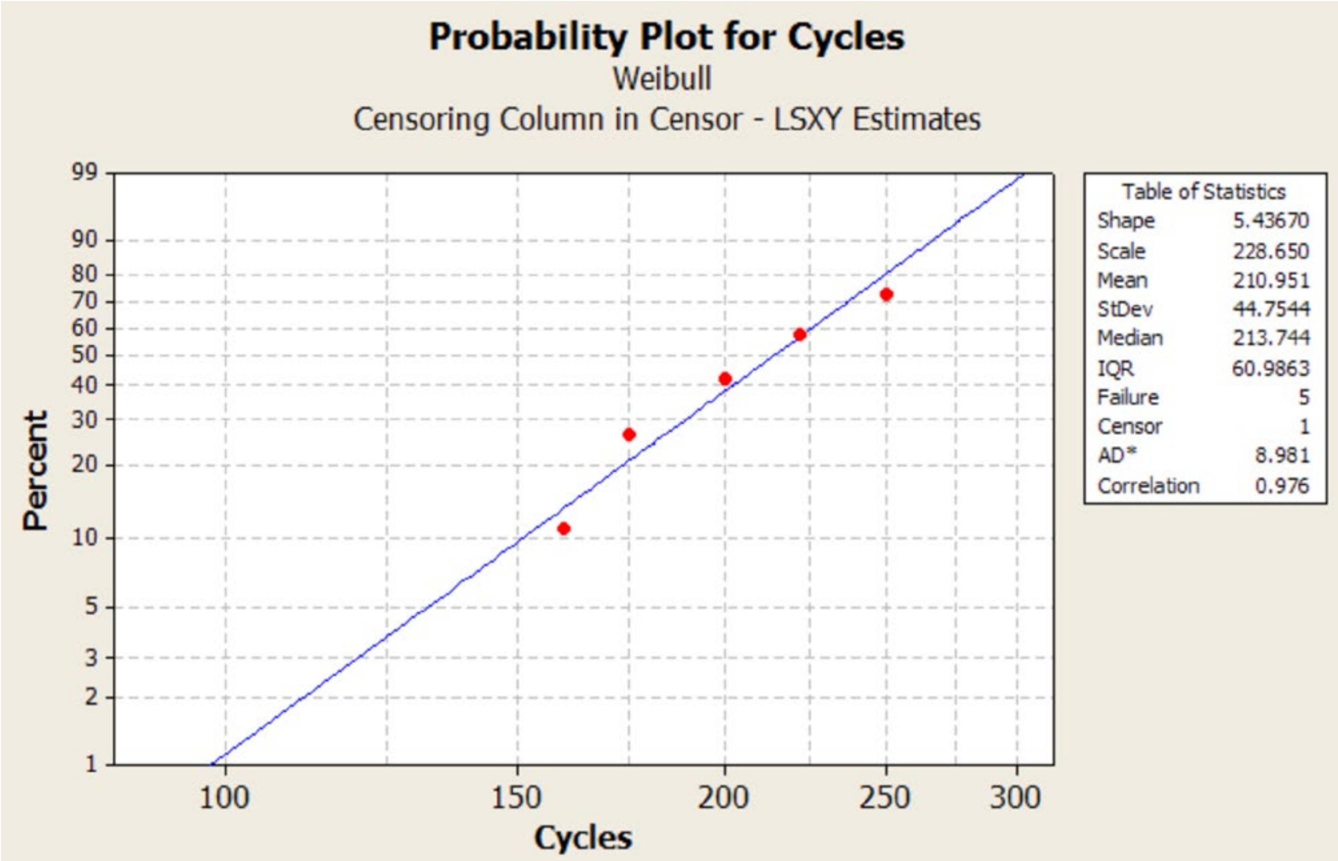

Figure 2: Weibull plot of the thermal cycle data from Table 2.

data set and then plotted. The percent (Y-axis) mimics the shape (β) parameter, with the scale (η) is at the 63.21% percentile. This is shown in Figure 3.

The beta (β) value is 5.4, indicating we're in the wearout zone of the product's life. If we're well beyond the design life of the parts, then we're happy. If we're within the design life, there is reason for concern as our parts are likely to fail during their useful life period.

Let's look at another example. In this case, we're in the lab and have formulated a new electroless copper and want to compare it to an industry standard. Test vehicles are processed through the new electroless copper and then subsequently finished in a printed circuit board shop. Results of the thermal cycling data are shown in Table 3.

As can be seen in table 3, there are no failures; all 10 coupons were censored at 1,000 cycles. Because we have good historical data on this coupon design, the shape (β) and the scale (η) are well known (3.43 & 580.5 respectively) so we can use Weibayes analysis on this data set.

Because we have no failures, the Weibayes analysis will give us a probability plot with only the lower 95% confidence interval. This can be seen in Figure 4.

Interpretation of the analysis is simple. The historical scale (η) is 580.5, and our new electroless copper scale (η) is 1,421.4 (95% lower bound), nearly

Cycles	Censor
1000	0
1000	0
1000	0
1000	0
1000	0
1000	0
1000	0
1000	0
1000	0
1000	0

Table 3: PTH thermal cycling data on new electroless copper.

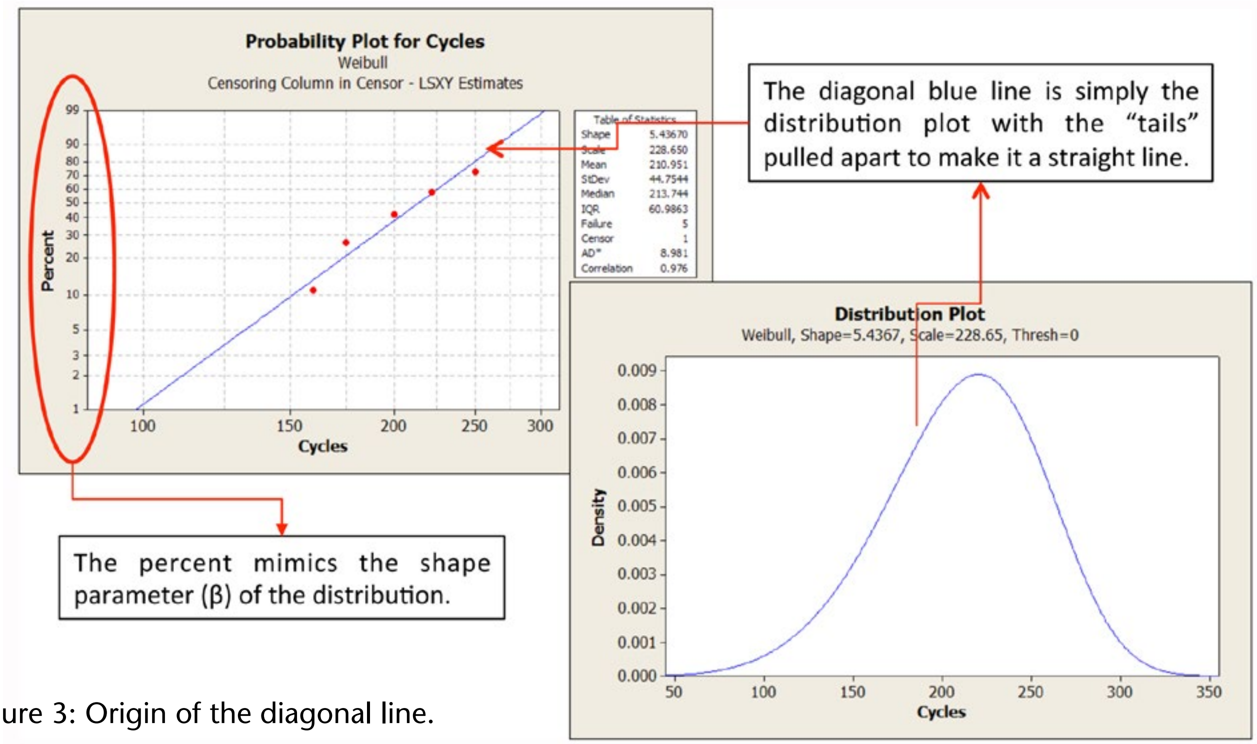

Figure 3: Origin of the diagonal line.

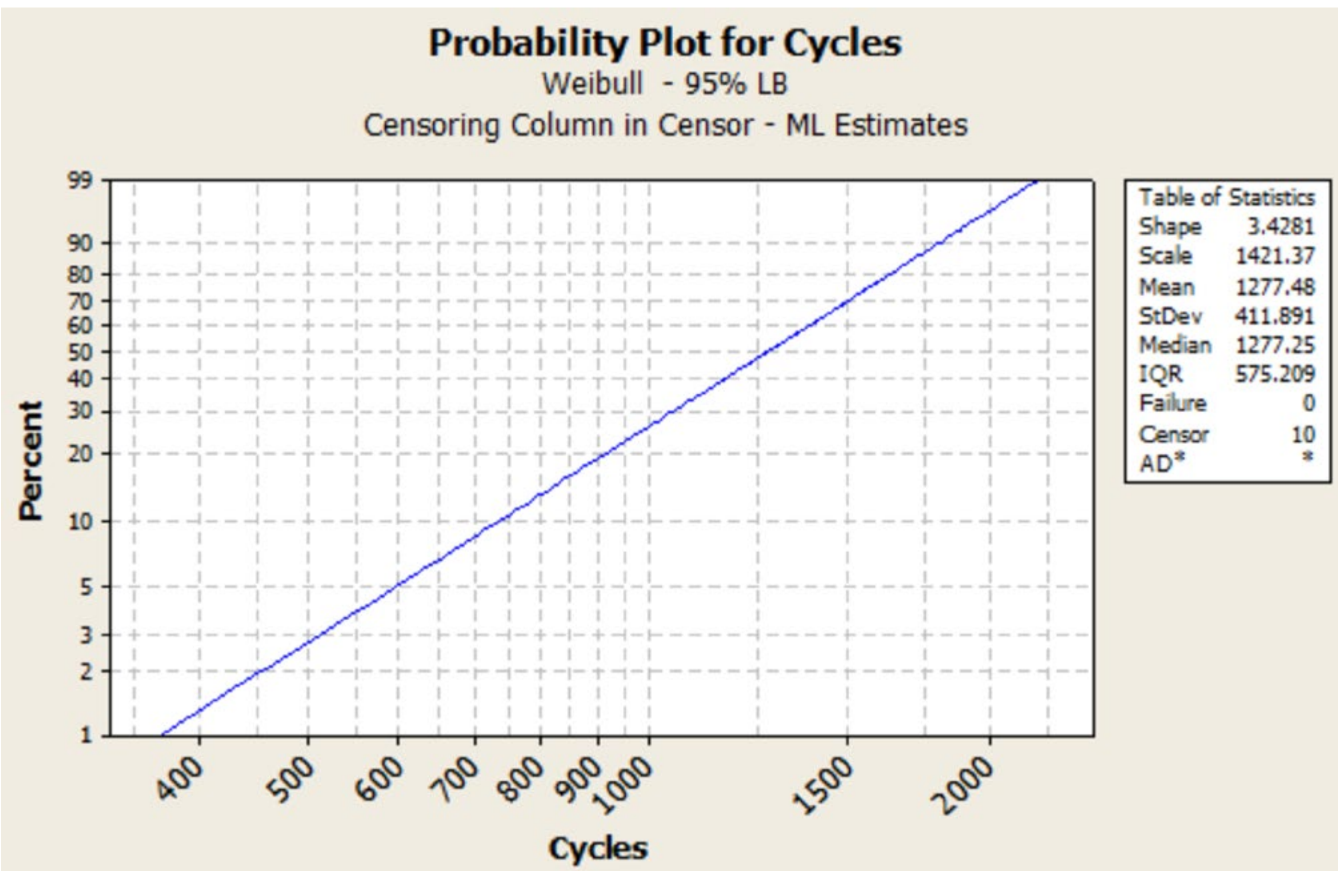

Figure 4: Weibayes analysis of Table 3 data set.

2.5x larger than the current industry standard process average.

As mentioned earlier, the challenge in reliability testing is correlating lab testing conditions to field use conditions. We know that temperature cycling causes thermal expansion and contraction that can induce mechanical stresses[10–14]. Let's define stress as force per unit area that results from an applied load, and strain as the physical deformation response of a material to stress. Stress is driven by the large differences in the coefficient of thermal expansion (CTE) between the plated through-hole copper and the laminate in the X, Y, and Z-axis. Stress relaxation and strain ratcheting occur during thermal cycling where tensile strength is reduced at peak thermal temperature, then increases as the electroplated copper is cooled. Cumulative strain then reduces elongation, and when the cumulative strain exceeds the critical strain, ductility exhaustion is reached and cracks occur. The faster the strain rate is applied, the quicker the critical strain is reached[14]. There are several failure theories used to explain these complex stresses; Von Mises stress has been used successfully[15], but in-depth discussion in this area is beyond the scope of this paper. Of interest are the CTE values of the electroplated copper and the laminate below and above T_g. Table 4 lists those CTEs; the laminate listed is a typical 180°C T_g material.

The coefficient of thermal expansion (CTE) is calculated as follows:

$$CTE = \frac{dl}{l \times dT}$$

Material	CTE
Electroplated Copper	17 PPM/°C
180°C Tg Laminate < Tg	45 PPM/°C
180°C Tg Laminate > Tg	230 PPM/°C

Table 4: CTE of electroplated copper and a typical laminate.

Where:

dl = the change in length of material in the direction being measured;

l = overall length of the material in the direction being measured;

dT = the change in temperature over which *dl* is measured.

We can rearrange the formula to solve for *dl:*

$$dl = l \times dT \times CTE$$

Let's look at an example of this by subjecting a 3.81 mm (0.150") thick printed circuit board to a thermal stress per IPC TM-650 2.6.8E. We're interested in the expansion above T_g, and in this case the laminate T_g is 180°C with a CTE of 230 (Table 4), and a solder temperature of 288ºC. We can calculate the Z-axis expansion as follows:

$$dl = 0.00381 \times 108 \times 230 \cong 95\mu m \ (3.7\ mils)$$

Calculating the out-of-plane elastic modulus is more challenging[16]. The result of the thermal stress is shown in Figure 5a. The mismatch of the CTEs causes significant stresses during thermal excursion, which is depicted in figures 5b and 5c.

With accelerated testing, we increase the level of stress (e.g., amplitude in temperature cycling, voltage, or pressure) under which test units operate. A unit will fail when its strength drops below applied stress. Thus a unit at a high stress will generally fail more rapidly than it would have failed at low stress; hence we have accelerated its life[10].

There are several different accelerated test models one can choose from. The Coffin-Manson relationship was originally developed as an empirical model to describe the effect that temperature cycling had on the failure of components in the hot part of a jet engine[10]. The Coffin-Manson model has been used successfully to model crack growth in solder and other metals due to repeated temperature cycling as equipment is turned on and off [12]. The generic form of this model is:

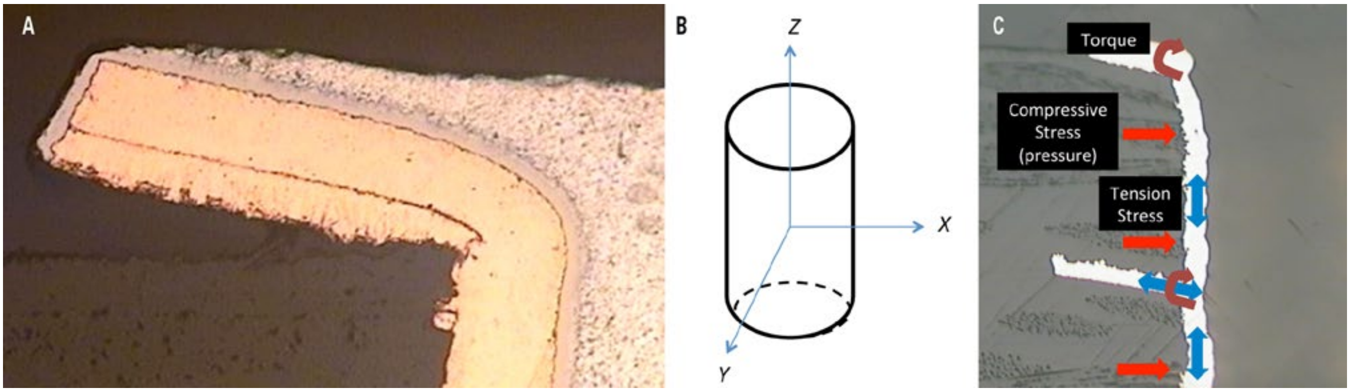

Figure 5a: Thermal stressed, pad rotation is evident. b: PTH stress axes. c: Thermal induced stresses.

$$Nf = \frac{\delta}{(\Delta T)^m}$$

Where:
Nf = Number of cycles to failure
δ = a material dependent constant
ΔT = entire temperature cycle-range for the device
m = an empirically determined constant

This power-rule relationship explains the effect that temperature range has on thermal-fatigue life cycles-to- failure distribution. General suggestions for m for ductile metal fatigue range from about 1–3[12, 17, 18, 19], and a critical review of a large number of papers led Blish to extract a useful set of m constants with copper listed as 5.0[19]. The acceleration factor for the test conditions is then derived by:

$$AF = \left(\frac{\Delta T_{Stress}}{\Delta T_{Use}}\right)^m$$

With low cycle fatigue (plastic strain), the acceleration factor is typically applied to the number of thermal cycles rather than the temperature exposure time[11]. Humidity is another commonly used accelerating variable, particularly for failure mechanisms involving corrosion and certain kinds of chemical degradation; however, humidity was not considered for this model. With high humidity, we would expect to see failures such as creep corrosion, whisker growth, and conductive anodic filament shorts (CAF). Escobar, Meeker, O'Connor, and Kleyner discuss and review several humidity models[10, 11]. Combined environmental stress testing (CERT) allows for the study of the effect of an interaction between two or more accelerated stresses, but it is generally not possible to develop an appropriate prediction model under CERT[1].

The IPC-TR-579 committee concluded that PTH reliability decreases as the thickness of the PWB increases, higher laminate T_g increase thermal cycle performance, and preconditioning the PWB (simulated assembly temperatures) reduces reliability[18].

Neumann, et al.[13], found a significant relationship between laminate T_g and PTH thermal cycling reliability. Laminate T_g significantly outweighed plated acid copper elongation for determining PTH reliability with the elongation varying between 15–25%. The researchers came to the same conclusion for the acid copper-plated thickness; that of the laminate T_g significantly outweighed the acid copper plated thickness for determining PTH reliability with the thickness varying between 20–40 micron. Thermal cycling was done both below and above laminate T_g.

Similar conclusions were demonstrated and reached showing reduced thermal cycling reliability of lower T_g laminates vs. high T_g laminates[20], and reductions in reliability were seen with larger deltas between the laminate T_g and peak thermal cycling temperature reached[7].

The goal of this paper is not to determine if a PWB design and material selection is appropriate for end use conditions as there are adequate models for this[18, 21], coupled with empirical data. The goal is to equate accelerated testing conditions to field use conditions. Looking at the Freda and Baker data[7], the worst case estimate of the T1% (1% cumulative failure) with 18 cycles at 245°C is 3,500 cycles to failure (CTF). Using the Coffin-Manson model with18 cycles at 245°C, and m ≈ 4.6 matches the cycles. Caution is needed, as the authors point out, because a difference of 1 or 2 cycles to failure is equivalent to 170 to 3,000 at thermal cycle temperature[7]. Based on this work, coupled with the m constant data compiled by Blish[19], m = 5 is a reasonable starting point for plated through hole modeling with the Coffin-Manson model.

Testing to failure was done at several different temperatures above laminate T_g and the data were used, along with research data, to generate an algorithm for estimating the m constant required for the Coffin-Manson model. Caution must be exercised when thermal testing exceeds the laminates T_g as failures modes can shift between interconnect defects (ICDs), electroplated barrel cracks, and laminate decomposition (carbonization), which can significantly underestimate the m constant. These defects are shown in Figure 6.

It's then relatively easy to input all parameters of the Coffin-Manson equation into a spreadsheet to simplify calculations (Figure 7).

Let's look at an example for a military avionics printed circuit board that has the following assembly, and anticipated harsh use field conditions[5]:

Assembly:	4x @ 245°C
Life expectancy:	10 years
Ambient temp:	20°C
Peak temp:	100°C
Power cycles:	1 per day
Total cycles:	4,467

Thermal cycling options:

1. 6x preconditions @ 260°C, 250 cycles at 150°C: Simulated cycles: 4,510

2. 6x preconditions @ 245°C, 300 cycles at 150°C: Simulated cycles: 4,571

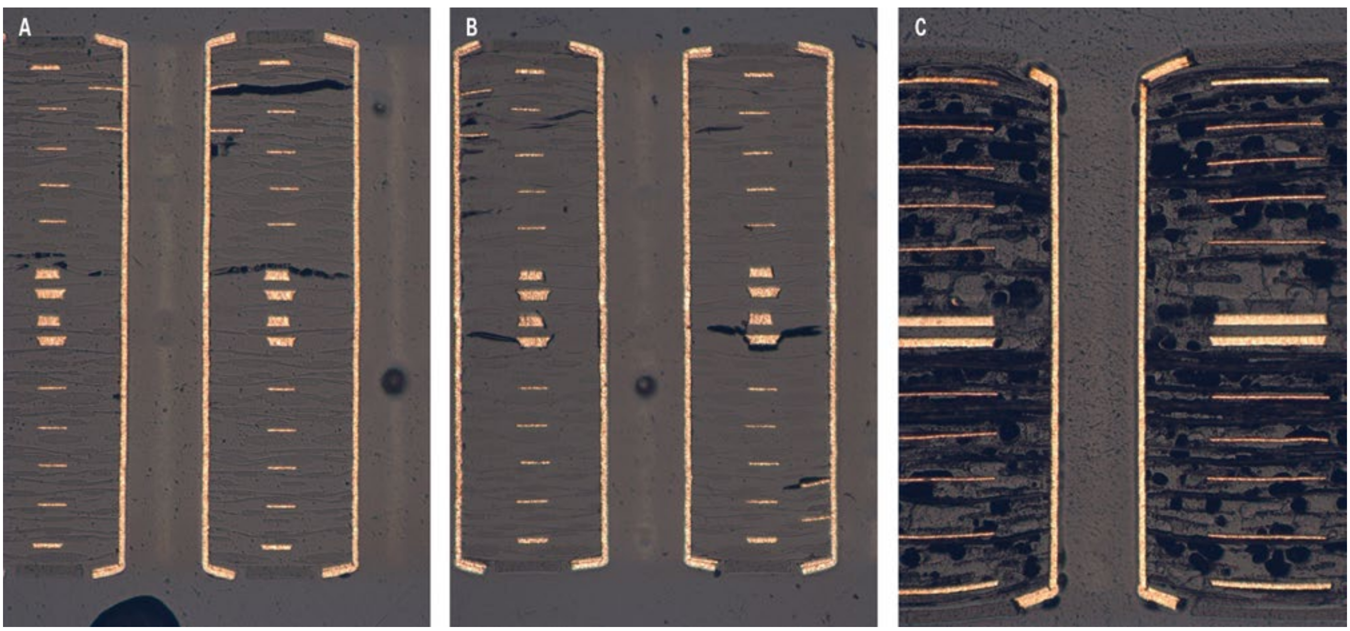

Figure 6: Testing to failure at 260°C. Note laminate T_g is 200°C. a: ICD failure 7. b: Electroplated copper crack at the knee. c: Laminate thermal decomposition (carbonization).

OM Group

Rev. 1PV

Thermal Cycling & Field Use Simulation

PCB Field Use Conditions

Life Expectancy Years:	20
Ambient power-off PCB temperature °C:	25
Operating power-on PCB temperature °C:	95
Cycles per day power-on/off:	1
Δ T:	70
Cycles per year:	365
Total Cycles:	7300
Subtotal Months:	240
Subtotal Years:	20

PCB Assembly Conditions

Reflow Cycles:	4
Peak Reflow Temperature °C:	230
Acceleration Factor:	2.73E+02
Total Cycles:	1,094
Subtotal Months:	36
Subtotal Years:	3
Total field cycles:	*8,394*
Total months of service:	*276*
Total years of service:	*23*

Thermal Cycling Pre Conditioning

Starting temperature °C:	25
Finishing temperature °C:	260
Pre-conditioning cycles:	6
Acceleration Factor:	6.01E+02
Simulated months of service:	118
Simulated years of service:	10

Thermal Cycling

Starting temperature °C:	25
Finishing temperature °C:	150
IST cycles:	300
Acceleration Factor:	2.29E+01
Simulated months of service:	226
Simulated years of service:	19

Parameter	Simulated	Field Use
Total Cycles:	10,489	8,394
Total Months:	345	276
Total Years:	29	23

Figure 7: Coffin-Manson equations in an Excel spreadsheet.

With a small sample size it may be more prudent to choose the lower preconditioning temperature as there will be less uncertainty in the simulated results.

Success (zero failures) and *success-failure* (a mix of successes and failures) reliability tests are based upon either nonparametric (binomial) or parametric (Weibayes) distributions. The well-known nonparametric binomial success testing sample size formula is:

$$n = \frac{ln\,(1 - C)}{lnR}$$

Where:
n = Sample Size
C = Confidence level
R = Reliability target

The *success-failure* testing sample size equation must satisfy the following relationship:

$$Bi(r; R_L, n) = 1 - C$$

Where:
Bi = Cumulative binomial distribution
r = Failures
R_L = Lower confidence limit
n = Sample size
C = Confidence level

To solve for n, one can use Goal Seek in Microsoft Excel.

Table 5 lists the 95% lower confidence limits for success-failure testing with user defined sample size and failures in the last row and column.

The general formula for parametric Weibayes sample size is:

$$n = \frac{X^2_{2r+2,1-C}}{2m^\beta\, lnR_L}$$

Confidence Level = 0.95	Sample Size																				
Alpha = 0.05		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	45
Number of Failures	0	5	22	37	47	55	61	65	69	72	74	76	78	79	81	82	83	84	85	85	86	94
	1		3	14	25	34	42	48	53	57	61	64	66	68	70	72	74	75	76	77	78	90
	2			2	10	19	27	34	40	45	49	53	56	59	61	64	66	67	69	70	72	87
	3				1	8	15	23	29	34	39	44	47	51	53	56	58	60	62	64	66	84
	4					1	6	13	19	25	30	35	39	43	46	49	52	54	56	58	60	81
	5						1	5	11	16	21	26	30	34	37	41	43	46	48	51	53	77
	6							1	5	10	15	20	25	29	33	36	39	42	45	47	49	75
	7								1	4	9	14	18	22	26	30	33	36	39	42	44	73
	8									1	4	8	12	17	21	24	28	31	34	37	39	70
	9										1	3	7	11	15	19	23	26	29	32	35	68
	10											0	3	7	10	14	18	21	24	27	30	65
	11												0	3	6	10	13	17	20	23	26	63
	12													0	3	6	9	12	16	19	22	60
	13														0	2	5	8	12	15	18	58
	14															0	2	5	8	11	14	56
	15																0	2	5	8	10	53
	16																	0	2	4	7	51
	17																		0	2	4	49
	18																			0	2	47
	19																				0	44
	20																				n/a	42
	0																					94

R_L listed in the table

Table 5: 95% confidence limits for the success-failure testing.

Where:
X^2 = Chi-square distribution
r = Failures
C = Confidence level
m = Constant
β = Shape parameter
R_L = Lower confidence limit

These calculations are easily done using software[9]. For example, we have a requirement to meet a R95C95 specification: 95% reliability (or probability of survival), with a confidence level of 95%, with a required time R(t) of 300 cycles. Historically, the Weibull shape parameter for this product type has been 4.29; we'll allow zero failures, and censor the testing at 500 cycles. Using Minitab®, we can calculate the sample size as follows:

Reliability Test Plan

Distribution: Weibull, shape = 4.29
Reliability Goal = 0.95, Target confidence level = 95%
Actual confidence level: 95.98%

Failures Allowed: 0
Testing Time: 500
Sample Size: 7

One caveat to consider is that parameter estimates result in sample size estimates, and when parameter estimates are based on a small sample size the confidence intervals can become wide, which can significantly under or over estimate the sample size.

There are a few general assumptions made about the proposed model when it is used to equate accelerated thermal cycling to field use conditions. Primary assumptions include that the thermal cycling coupon is representative of the PCB in terms of design, PTH quality (drill, desmear, glass exposure, copper plating thickness, etc.), out-of-plane dimensional movement, and workmanship. It's well established that the quality of the PTH has a significant impact on reliability[15, 16, 18], and that the thermal cycling test conditions, with the failures they induce, represent the field use failure mechanisms. The model itself is conservative by nature and the higher the peak testing temperature is above the laminate T_g the more uncertainty there is about the results as the m constant may be significantly underestimated. For thermal testing above T_g the model has a strain component, and below T_g thermal cycling the model accounts for strain ratcheting, with the m constant being empirically derived. For thermal cycling temperatures below ~140°C, empirical work would be needed to determine the m constant. The model was built around laminates in the 170–200°C T_g and may not be appropriate for other laminate T_g ranges. However, the goal is not to determine if a particular design is reliable, it's simply to equate lab testing to field use conditions. Humidity was not considered in this model, and it's well known that moisture within the laminate will volatilize during thermal excursions. It's assumed that the thermal cycling test coupons are handled and stored properly before testing; industry-recognized standards make no mention of pre-baking test coupons[22], but several OEMs have written their own testing protocols which include pre-baking of coupons prior to thermal cycling testing. As George Box said "…all models are approximations. Essentially all models are wrong, but some are useful. However, the approximate nature of the model must always be borne in mind."[23].

Once thermal cycling data is completed, failure analysis is in order. This should include distribution fitting, data exploration, reliability analysis and interpretation, and statistical process control.

Conclusions

Reliability testing has evolved over the last 100 years with significant improvements in accelerated testing methods and sophistication in data analysis; having an understanding of reliability terms and methods is important. Work is still needed in reaching industry consensus as to what each of the reliability test protocols prove and when each test protocol should be used. Correlating laboratory accelerated testing to field use conditions is challenging and can be misleading when test conditions are too extreme, as the acceleration interval becomes excessively wide, which can significantly under or over estimate reliability. When thermal testing temperature approaches the failure threshold, significant variability is introduced, and larger sample sizes are recommended. Future work will focus on refining the acceleration factor and correlating accelerating testing to field use conditions.

The author wishes to acknowledge and give thanks to Viola Richard, OM Group, for her work in running all the thermal cycle testing and cross section work, and Dr. Thomas P. Ryan for his review of the paper and his critiquing of the plausible Coffin-Manson fatigue model to correlate accelerated thermal cycling test conditions to printed circuit board assembly and field use conditions. **PCB**

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VIDEO INTERVIEW

Sanjay Hupikar and Dan Feinberg Discuss IPC APEX EXPO 2015

by Real Time with... IPC APEX EXPO 2015

The 2015 event had higher attendance and in general many exhibitors seem happy with the quantity and quality of those attending. Sanjay also discusses the increased membership as well as the IPC global efforts. Of particular interest is his vision for the newly formed Ambassadors Council and its new mentoring efforts. The locations for the next four APEX EXPO shows were also confirmed.

realtimewith.com

Thermal Management for LED Lighting Applications

by Les Round
SPIRIT CIRCUITS

PCB substrates designed for thermal management have been around for a number of years, traditionally servicing power-related applications; however, there are now many more suppliers and substrates emerging to meet the growing demand from LED lighting products. The LED package emits light forward and any excess heat is designed to be dissipated from the base of the component, usually through a bespoke thermal pad or through either the anode or cathode pads. Like other electronic components, the failure rate of an LED doubles with every 10°C increase in junction temperature. So based on the fact that reliability and longevity are key requirements for the successful uptake of LED lighting, good thermal management is an essential element in this growth.

A wide range of available LEDs put varying thermal demands onto the PCB substrate. Low-wattage (0.25W LEDs) and low-density applications are typically dealt with by using standard, single-sided FR-4 or CEM PCBs, where all the heat must be dissipated at the surface and the thermal performance is enhanced by using large copper lands (for heat spreading) and higher copper weights when required. The FR-4/CEM materials are very good thermal insulators and so obtain little or no benefit from a secondary heat sink and the operating temperature is directly influenced by the ambient temperature and although this does limit the use of this technology, it still represents a significant part of the LED market. It should be noted that there are some new FR-4/CEM style laminates that have been developed with a higher thermal conductivity, which allow the LEDs to benefit from secondary heat-sinking.

For mid-power (1.0W LEDs), moderate density applications, where the thermal requirements are beyond the capability of a standard, single-sided PCB, the next level of thermal performance comes from FR-4 PTH PCBs using thermal vias to enhance heat dissipation. The heat generated by the LED spreads across the pad and then down the plated via holes to a large copper area on the other side of the board, OM Group

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Outer Layer

TECHNOLOGY

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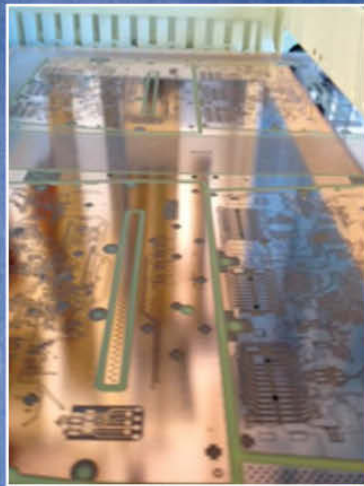

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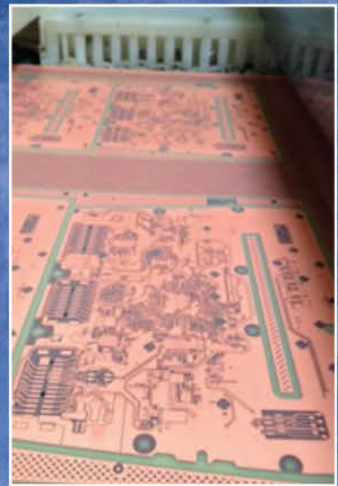
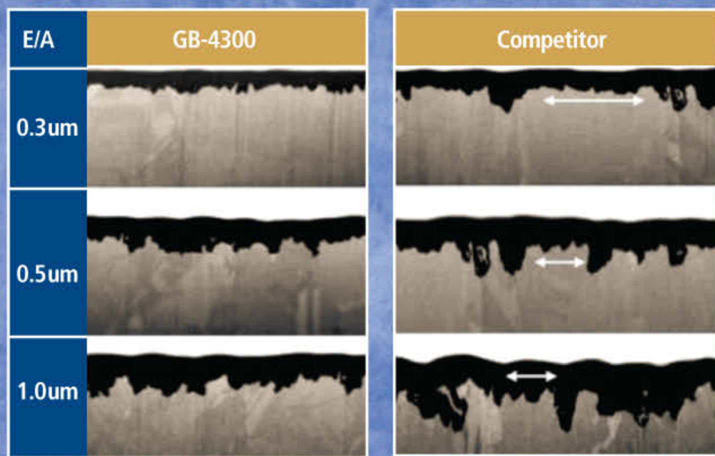


After GB-4300

Copper Roughening Process for SM & IL Adhesion Promotion

Lower Profile for Signal Integrity and Final Finish Appearance



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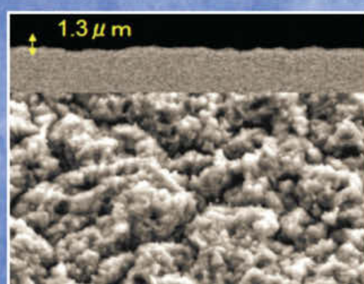
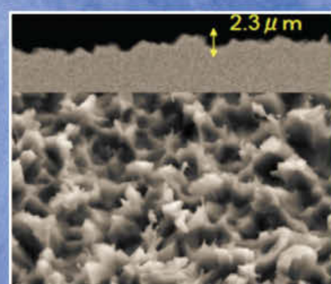
- Lower etch amount required than competitive processes



GB-4300



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this heat can then be dissipated into a secondary heat sink. The holes around the LED pads do limit the potential LED density, and from our experience we find that holes placed further than 5 mm from the LED have a much reduced effect on the junction temperature. Obviously, the use of via-in-pad technology will allow for higher LED packing densities but this does create other assembly issues (and if this means using hole-filling, then any cost-savings for using FR-4 will be eroded); however, via-in-pad will improve the thermal performance when compared to having vias around the LED (Figure 1). To obtain the maximum thermal performance from this PTH approach will require the use of an isolating thermal interface material (TIM), which will eliminate the risk of electrical leakage and help considerably with heat dissipation (into a secondary heat-sink). Ideally, the non-LED side should have no solder resist coating as this provides the best transfer of heat (i.e., using the TIM to provide the electrical isolation); however, many applications use a solder resist in order to ensure the PCB is electrically isolated from the heat sink.

When it comes to mid- to high-power or high-density LED applications, many companies turn to insulated metal substrates (IMS) because it provides a convenient and reliable thermal solution as it comes with an in-built heat-sink (Figure 2). The IMS is a relatively simple material which comprises of a copper foil bonded to a metal base with a thin dielectric. The copper foil provides the circuit image, and because the heat dissipation is primarily routed directly through the dielectric, then the copper weight is less of an issue (as with FR-4 products) and this helps when tracking high-density designs. The metal base is usually aluminium because of its light weight and relatively low cost, and because it is a well-established heat-sink material (thermal conductivity 140–200 W/mK, depending on the grade). For more demanding applications, copper is used (thermal conductivity ~400 W/mK) even though it is heavier and more expensive. It is in the dielectric layer where we see the main difference between suppliers (and their product range), although they all tend to be thin layers (sub 0.20 mm) with a varying level of thermal properties. Typically, the thermal performance of these dielectrics is enhanced by the addition of ceramic materials (such as aluminium oxide, aluminium nitride and boron nitride), increasing the thermal conductivity of the base resin from around 0.25W/mK to upwards of 5W/mK. Most LED applications are low voltage systems, so electrical breakdown performance is not normally a major concern, although most of the

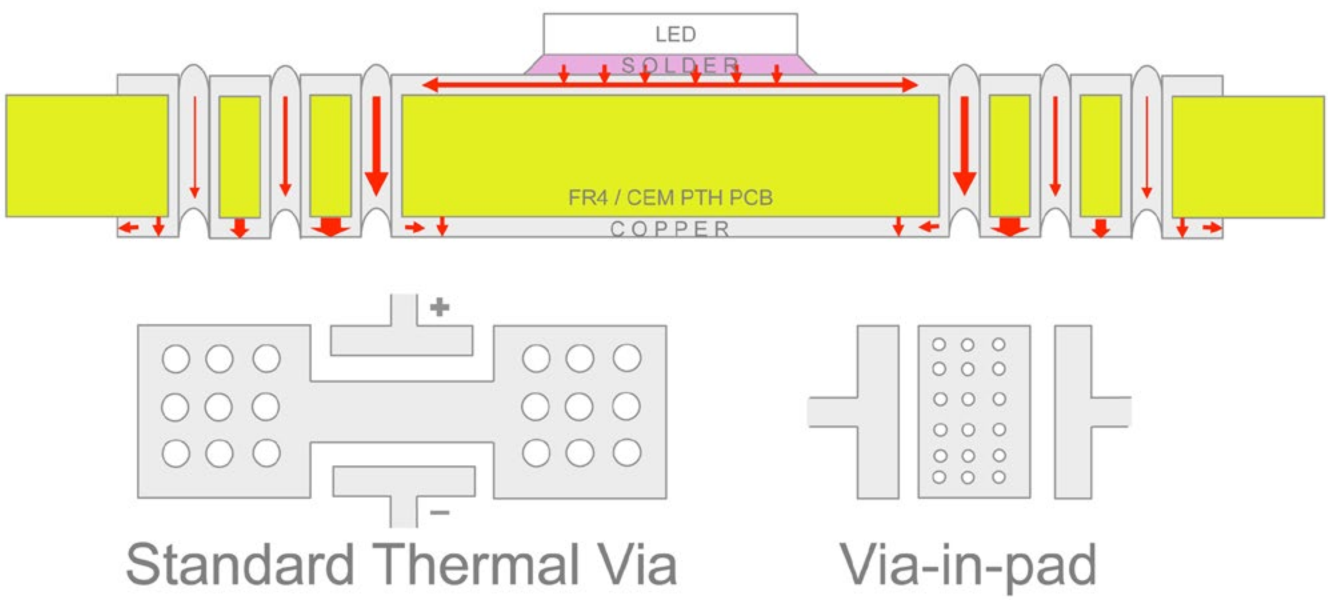

Figure 1: FR-4/CEM PTH using thermal vias.

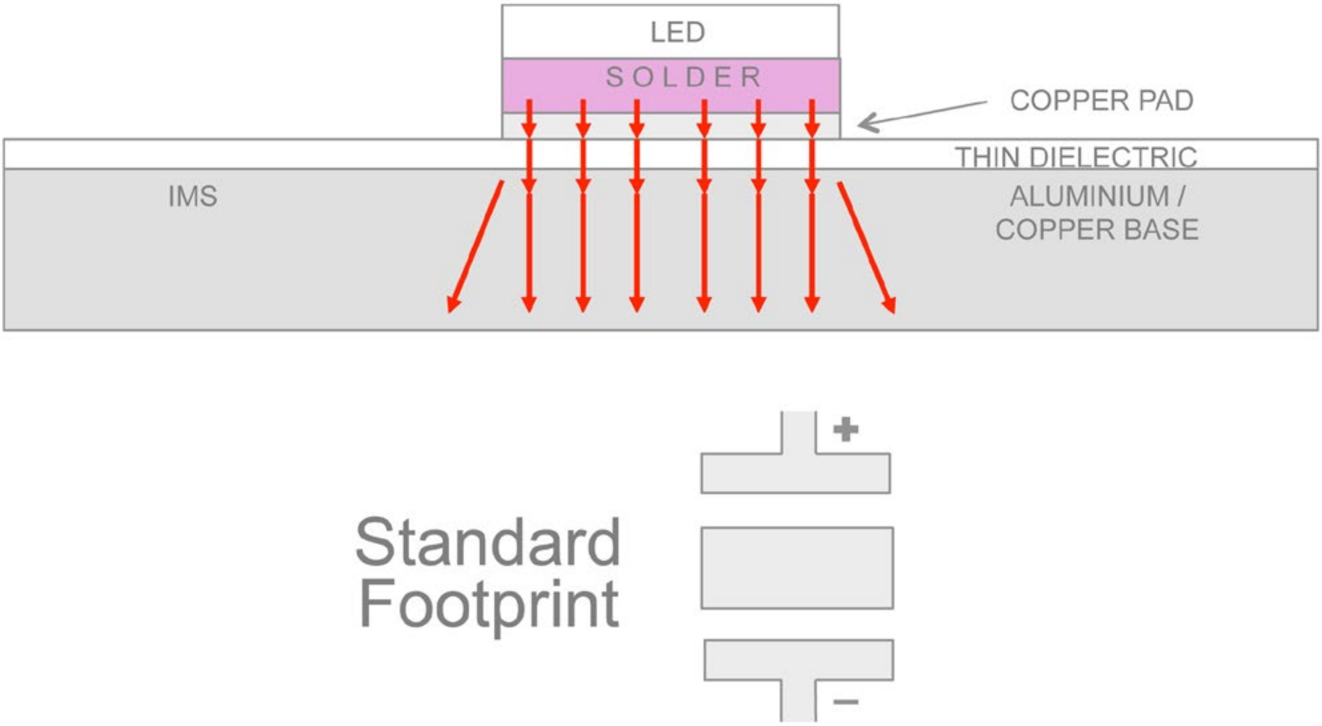

Figure 2: Standard IMS MPCB.

materials on the market will easily withstand 1000V DC (and most will withstand 3000V).

When selecting an IMS for a particular application, most companies seem to select based on the claimed thermal conductivity; however, it is better to select based on the thermal impedance, which is basically the relationship between the thermal conductivity and the thickness of the dielectric. This is, more or less, a linear relationship, so if the thermal conductivity is doubled, or if the thickness is halved, then the thermal performance is improved by a factor of two. This fact is used by some suppliers offering dielectrics that have no ceramic fillers but are very thin (e.g., 25 microns) in order to maintain a good thermal performance; and there is also a trend for thin, ceramic-loaded materials that are providing superior thermal performance (i.e., very low thermal impedance).

As demand increases, new materials are continually appearing, with one in particular that is aimed strictly at the high-performance sector. This material differs from the standard IMS because the ceramic is actually deposited directly onto the aluminium base, providing a thin dielectric layer coupled with a high thermal conductivity, resulting in a very low thermal impedance substrate. Formable versions of IMS are also available, and they are similar in appearance and construction. They use rolled and annealed copper foils, thin, non-reinforced dielectrics, and a malleable grade aluminium, all designed to bend without cracking.

As mentioned previously, many customers select materials using the thermal conductivity as stated on the technical data sheets (TDS); however, from evidence gained during simple product evaluations it would indicate that this information should only be used as a guideline, as materials often with similar stated thermal performance appeared to perform differently when tested under similar conditions. Originally, the in-house product approval test at Spirit Circuits used a PCB made from the material to be tested, with a simple star design. A standard LED was attached, with a thermocouple connected to its thermal pad, and its temperature was logged over a range of drive currents (100, CP 6080

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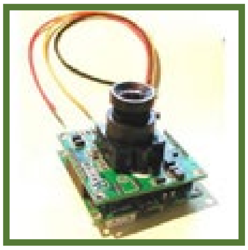

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350, 500, 700, 1000 & 1200mA). The results were then compared to similar materials currently being used, and although this was not exactly a scientific approach, it was observed that TDS information was not always accurate when comparing materials (based on junction temperature). Note: The differences observed with TDS performance figures may be due to the various test procedures used and some figures maybe based on theoretical calculation.

Another test programme included the building of equipment capable of accurately and consistently testing the thermal performance of IMS materials. It was decided to adopt a similar technique used by one of the well-established IMS manufacturers and this involved using a TO-220 device under a controlled load as the heat source. A standard sample tile of the IMS is located onto a temperature controlled heat-sink (which maintains a constant temperature during the test cycle); the TO-220 is clamped onto the IMS and the temperature of the top and bottom of the IMS monitored until the TO-220 junction temperature remains constant (Figure 3). The thermal impedance for each material could be calculated using these test results and these results are now used to select the best material for a particular application based on performance and price (always a key element for LED lighting products). The equipment can be used to test the effectiveness of TIMs, heat sinks, expected operated temperature of a luminaire, etc., as well as being a standard test method for testing new IMS materials.

As IMS materials become more widely used and understood, alternative ways of incorporating this technology into other, non-standard constructions has increased and these include metal-core and hybrid builds (i.e., PTH or multilayer boards bonded to a metal heat-sink using ceramic-loaded prepregs).

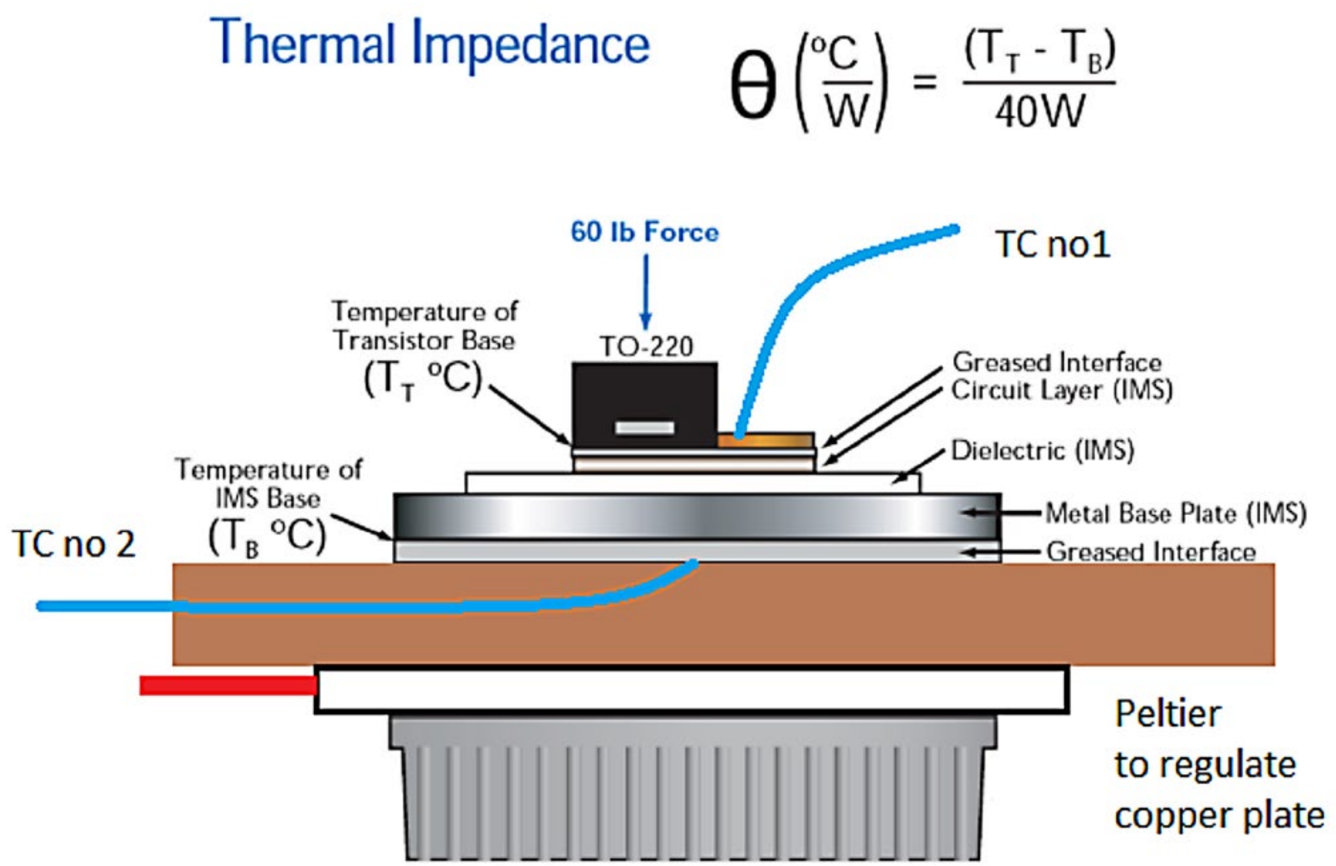


Figure 3: Thermal impedance test equipment. (Source: Spirit Circuits)

As a general rule, IMS selection should be based on the specific requirements and use of the intended product. For example, high performance, premium IMS materials are very useful for down-lighters and will generally provide a lower operating temperature; however, you only gain the benefit if the associated heat-sink will dissipate the heat, so the heat sink must not already be at saturation point). Also, for applications that require long warranties (e.g., tunnel lighting), or are difficult to maintain (e.g., oil/gas rigs), it may be advisable to use an IMS even when a FR-4 option is acceptable, because generally, they will provide a reliably lower operating temperature (as they rely less on any secondary heat-sinking).

Interestingly, recently one of the major LED fabricators also suggested that LED lighting manufacturers should review the overall system cost instead of focussing solely on the cost of the LEDs. They indicated that the improved reliability of the new generation of LEDs could be utilised by operating them at higher temperatures (by using smaller heat sinks and/or PCBs) and still obtain an acceptable product life. So adopting this approach would also form part of the selection criteria used for material selection. Although this will no doubt be helpful for some applications, there are also many situations where low density (and even large format) PCBs are used primarily to eliminate LED 'spotting'.

Even though LED technology improvements are making them more efficient and generate less thermal issues, they still present a range of thermal challenges on materials in order to provide the reliability and longevity the market expects and demands.

In summary, when selecting the best material and technology for a specific application, it should be done based on a thorough understanding of the application, including: luminaire design; any heat-sinking; TIMs; whether is it potted; maintenance requirements and warranty issues). It is critical to be involved at the early stages of design so that the optimum PCB layout, size, material, performance and cost-effective solution may be selected. **PCB**

Les Round is technical sales manager at Spirit Circuits.

EIPC Honors Starkey and Ling as Valued Industry Fellows

At the 2015 EIPC Winter Conference in Munich in February, EIPC Chairman Alun Morgan (l) praised the efforts of two people, John Ling and Pete Starkey (r), by presenting both with a plaque proclaiming their Honorary Fellowship, which had been conferred by the EIPC in recognition of their loyal support and outstanding contribution to the PCB industry over many years.

John Ling has been involved with the EIPC for many years and is the erudite editor of the EIPC's SpeedNews, amongst other activities in support of the institute.

Pete Starkey is a member of the EIPC conference programme committee and is the distinguished editor of many EIPC conference and workshop reviews. He also serves as technical editor for I-Connect007 publications.

Both gentlemen also provide technical support to the EIPC for the many EU funded projects initiated from Brussels.

Regarding receiving the award, Starkey said, "It was totally unexpected and Ling and I were both totally flattered by the gesture. It's been an absolute pleasure to be of service to the EIPC, and to work with such a distinguished organization."

The EIPC Summer Conference will be held June 18 & 19 in Berlin. For more information, click here.

Mil/Aero007
News Highlights

Over a Dozen RoHS Exemptions Requested

IPC, in conjunction with an international industry stakeholder group, applied for more than a dozen exemption extension requests under the European Union (EU) RoHS Directive. The RoHS2 Directive dictates expiration dates for all exemptions granted and several critical to the electronics manufacturing industry are set to expire in 2016.

A Cautionary Tale: Counterfeit Materials

John Ling of EIPC writes, "Risk from counterfeits wears many hats. There is reputational risk, which can be damaging; there is inherent safety risk, which could be fatal; and there is financial risk to the OEM, the PCB manufacturer, and the PCB broker. One way of minimising risk is by dealing direct."

DARPA Boosts Investment in LRASM Program

Initiated in 2009 in collaboration with the U.S. Navy and U.S. Air Force, DARPA's Long Range Anti-Ship Missile (LRASM) program has been investing in advanced technologies to provide a leap ahead in U.S. surface warfare capability.

FTG Secures New Agreement with Rockwell Collins

The agreement incorporates a variety of technologies for use on major airframe platforms across business regional, air transport and government systems market applications.

DARPA to Put Fab Lab at Navy Ship Maintenance Center

High-tech fabrication facility aims to enhance ship maintenance and repair by enabling more cost-effective training and rapid onsite production of parts and components.

Camtek Secures First Conditional Order for Gryphon

Camtek Ltd. announced that it has received a conditional purchase order from Bay Area Circuits Inc. for a Gryphon system. The purchase order will become firm upon successful completion of an evaluation process.

It's Only Common Sense: Saving the Military PCB Market

The DoD has to come to its senses and start working with the sub-$20 million well-qualified board shops. These shops have been the backbone of the American PCB industry since its inception. It must work with them and support them, making sure they pay prices that are fair enough for them to stay in business.

New Defense PCB Regulations Take Effect December 30

Changes to the U.S. Munitions List, which is regulated through the International Traffic in Arms Regulations, states that PCBs "specially designed" for defense-related purposes will be controlled under USML Category XI. Additionally, any designs or digital data related to "specially designed" PCBs will be controlled as technical data.

2015 Global Aerospace and Defense Industry to Rise

"The commercial aerospace sector is expected to set new records for aircraft production in 2015. The accelerated replacement cycle of obsolete aircraft with next generation fuel-efficient aircraft, and growing passenger travel demand, especially in the Middle East and the Asia-Pacific region are key drivers behind this trend," said Tom Captain, Deloitte Global Aerospace and Defense Sector Leader.

IDTechEx Sees Rapidly Changing $7.5B Market for Drones

Dr. Harrop, Chairman of IDTechEx says, "The biggest market sub-sector will be small UAVs that are not toys or personal, with $2 billion in sales in 2025 generating over $20 billion in benefits to agriculture, border protection, parcel delivery, logistics such as warehousing, coastguard, customs, search and rescue, medical emergency, malaria research, mine detection, protection of rare species, movie production and so on."

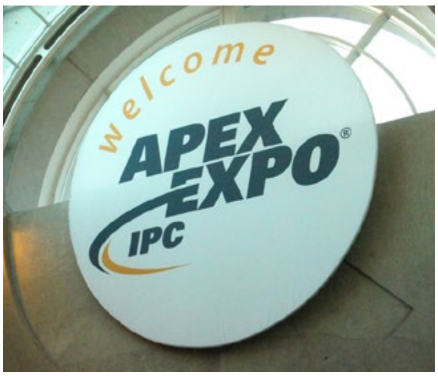
San Diego Convention Center, San Diego, California, USA

IPC APEX EXPO 2015: Tough Act to Follow

by Joe Fjelstad
SPECIAL TO I-CONNECT007

Based on personal impressions and conversations with folks met on the show floor and technical meetings, this year's IPC APEX EXPO trade show and conference was an unqualified success. The various trade show, conference and standards committees, in concert with the IPC staff, continue to raise the bar, improving the event to the benefit of members and industry participants from around the globe.

However, this year also marked, with sorrow, the first IPC APEX EXPO at which much beloved IPC staff member and industry icon, Dieter Bergman, was absent. It was tough not seeing him at the event—a feeling that was shared by everyone I met. Yet somehow, I sensed that many might have felt, as I did, that Dieter's spirit was still with us, urging us on.



In that regard, one of the highlights of APEX for me this year was an event held on Wednesday evening. It was a special tribute honoring Dieter with shared remembrances of a man, the likes of which we are unlikely to see again in our lifetimes. The well attended event was also the inauguration of the Dieter Bergman IPC Fellowship award. This new award in Dieter's memory was bestowed upon on a group of highly respected veteran IPC volunteers, each with decades of service to IPC and the industry. The inaugural award recipients included: Doug Sober, Shengyi Technology; Bernie Kessler, Bernard Kessler Associates; Denny Fritz, SAIC; Dave Hillman, Rockwell Collins; Don Du Priest, Lockheed Martin; Bob Neves, Microtech; Ray Prasad, Ray Prasad Associates; and Randy Reed, Via Systems. Each recipient was allowed to bestow a Dieter Bergman memorial scholarship upon the college or university of their choice. It

was a fitting tribute for a man who spent most of his life in service of and teaching industry colleagues around the globe.

Another highlight of the week was the induction of Gary Ferrari to the IPC Raymond Pritchard Hall of Fame. Ferrari was the first executive director of the IPC Designers Council and was instrumental in organizing and structuring the training courses that have been the backbone of design instruction for entry level PCB designers as well as the certification of seasoned ones.

A couple of other items of note caught my interest and attention. The first was a significant departure of tradition. This year's keynote session had a sponsor, eSurface. The company presented an impressively produced video which provided a visually captivating overview of their novel circuit manufacturing technology. Doubtless, it caught most everyone off guard. It was a foray into new territory for IPC and a significant break from tradition; frankly, I like such experimentation and the breaking of traditions. It could presage a future when, like the Super Bowl, such commercial productions, if done to a similar high level as this first one, could prove of as much interest to attendees as the subject of the keynote.

Finally, on the morning of the last day, there was the inauguration of IPC Town Hall, an open event, the purpose of which was to engage senior staff members, including president and CEO John Mitchell, directly with members in attendance with the intent of creating a dialog relative to what might be missing and or improved on with IPC programs and services. Discussions were lively and the challenges discussed were both real and important. I look forward to attending future such events. I think it could prove a great way for frontline members of IPC to express their desires and needs and hopefully help guide the association to improve its services to both members and the electronics industry.

In many ways new and old, the 2015 IPC APEX EXPO is going to be a tough act to follow. **PCB**

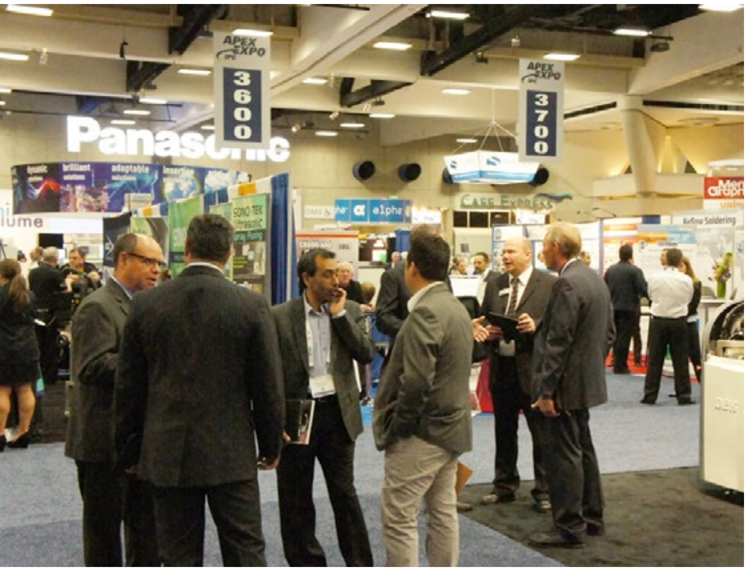
This Ice Cream's for You, Dieter

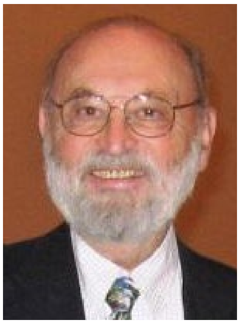
by Patty Goldman
I-CONNECT007

Another year has come and gone and so has another IPC conference and show. Doesn't seem that long since the last one, but a year is a year (well, actually 11 months but who's counting).

I'm one of those cross-over people, involved in committee meetings, the technical program and also an exhibitor at the show. San Diego is such a great venue for this, with everything right there and accessible. How pleasant to be able to quickly transfer from one area to the other. Plus, you were just a few steps from the door and could step out into the sunshine and perfect weather at any time; there were even tables set up outside (in the back) that we could use. We sure missed that in Las Vegas!

A number of people mentioned that everything seemed so…organized. The technical conference ran smooth as silk (at least that's what we saw—I know IPC staff works hard at that). Same comment for the show and show floor. It's always amazing to see the transformation from Monday night to Tuesday's opening bell. But it was really all very organized. The technical conference session I moderated was pretty much packed. The show floor was very busy on Tuesday, a little less so on Wednesday, and Thursday was exhibitors' day—where the exhibitors have a chance to conduct business with each other. I am sure much was accomplished all around.





A most notable exception to the regular programs was the tribute to Dieter Bergman on Wednesday evening. Dieter was without question the most recognized and best known person at IPC, truly the face of IPC. While most knew of him, recognized him, perhaps had met him or heard him speak, some of us were better acquainted with Dieter. We worked with him on standards activities, argued with him, had dinner and ice cream with him, laughed and argued some more, and counted him as a true friend. Many people spoke on Wednesday evening, recounting funny stories and jokes. But all had another common thread—friendship.

After this event a group of us decided on another IPC meeting tradition: ice cream! We headed out with IPC patriarch Bernie Kessler to a tiny shop in the Gaslamp District. Some of us had gone on many an ice cream outing at IPC meetings; we dragged along some newbies this time. The only rule was "no business to be discussed." And so a pleasant hour was spent and new friendships were formed, complete with the required group photo (thanks, Kelly Dack). And that's what it's all about. **PCB**

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Real Time with...IPC APEX EXPO 2015

An Interview with Keynote Speaker Dr. Stanton Friedman and Publisher Barry Matties

After Wednesday's keynote, publisher Barry Matties invited Dr. Stanton Friedman, a nuclear physicist, lecturer and UFO researcher to the *Real Time with...* booth for a lengthy interview on Friedman's long career with companies such as GE, Westinghouse, and McDonnell Douglas, among others. Friedman has worked extensively on highly advanced and classified programs focused on nuclear aircraft, fission and fusion rockets and compact nuclear power plants for space and terrestrial applications. Friedman has presented at more than 600 colleges and universities and 100 organizations spanning the United States and Canada, and more than a dozen countries abroad. The following is excerpted from the complete interview conducted on February 25, 2015 on the show floor.

On ENERGY RESEARCH:

Barry Matties: I'm interested in how your career and our industry eventually intersected. Let's start by telling us about your early career, and the scope of your work in energy programs.

Stanton Friedman: From 1956 to 1959, I worked on the General Electric aircraft nuclear propulsion program at Cincinnati General Electric. In '58, we spent somewhere around $100 million. We employed 3,500 people, of whom 1,100 were engineers and scientists. In other words, it wasn't six professors and 12 grad students; it was a major effort to develop a nuclear airplane that could fly farther, longer. It wouldn't have to stop for fuel. All the programs that I worked on spent tons of money. It was all based on the premise that we were going to beat the Russians.

When I worked for Westinghouse, we tested a nuclear rocket engine that was less than eight feet in diameter. The power level was 4,400 megawatts, twice the power of Hoover Dam, which is a little bit larger than that. It was all government funding. Then they cancelled the program. It takes guts to pursue new technology.

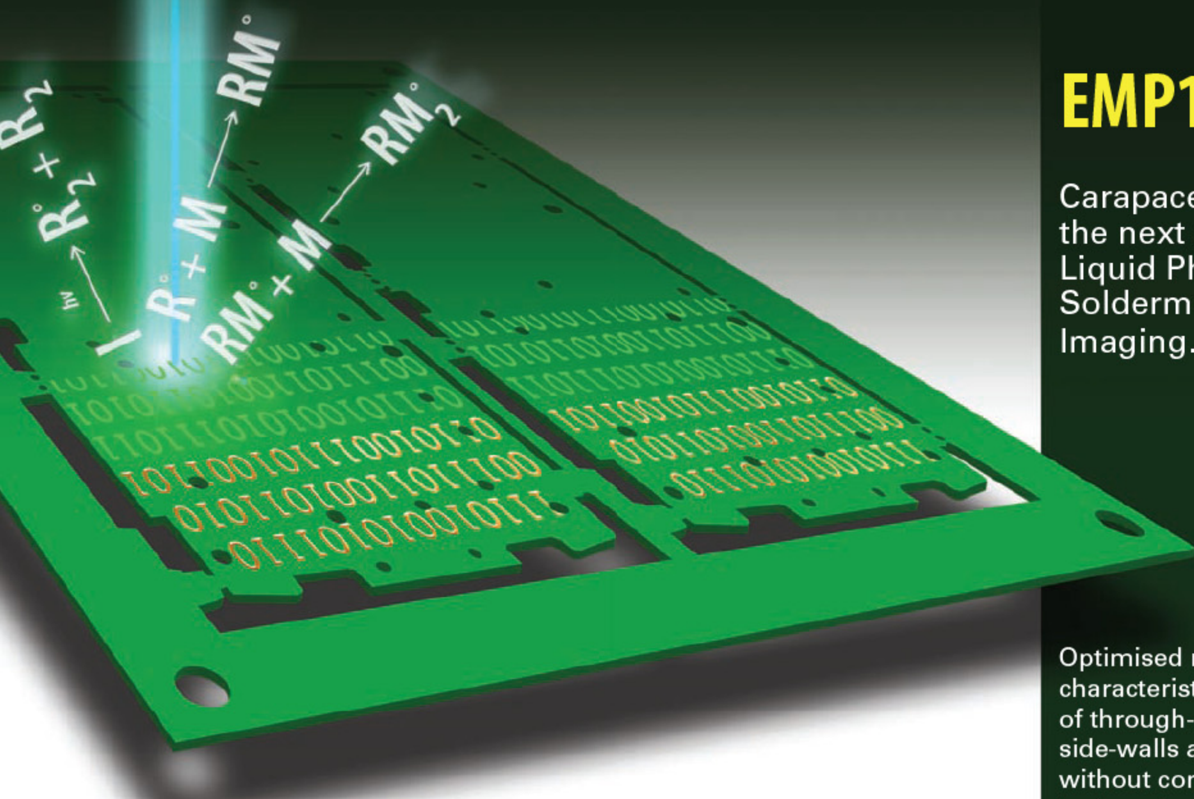
Barry: There is such a fear of nuclear energy as a power source, which I don't understand.

Stanton: I don't understand it either. Nobody said, "We should get rid of all our cars because we killed over 30,000 people last year with automobiles." That's the price you pay.

Barry: I understand the catastrophe we saw in Japan, but now my understanding is, and maybe you can clear my thinking up here, that years ago the French approach was not to use rods, but balls, it seems. They turned off all the cooling. There was no melt-down.

Stanton: The nuclear industry is frankly one of the safest industries. I'm not an apologist for the industry at all. I belong to the American Nuclear Society who use double, triple, quadruple backups for things because they realize how important it is. If you're in a submarine, often in the middle of nowhere and down 1,000 feet, the alarm system better be reliable. It isn't

Direct Image Solder Mask



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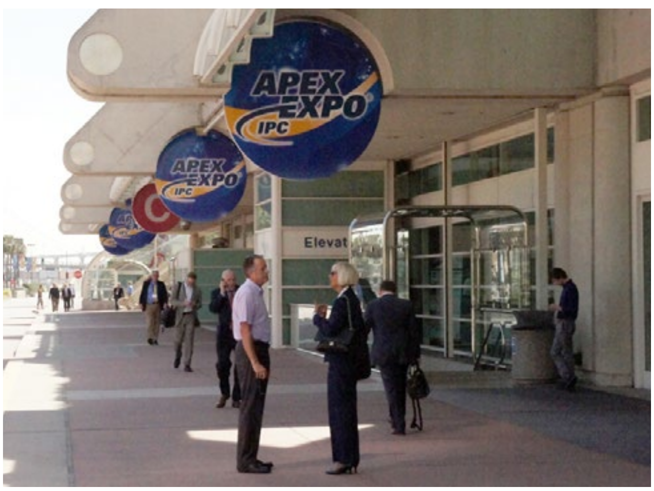
enough to say, 'It works but if something goes wrong, we'll just stop in a port and fix it.' It's not like you're driving on the highway and you need a new tire or a new battery. You're shit out of luck if these things don't work reliably.

They're designed for long life but people are shocked when I tell them, 'We have nuclear power to aircraft carriers that can operate for 18 years without refueling,' which means everything in there has to be ultra-reliable. What good is it if things break down all the time?

On TECHNOLOGY:

Barry: What is your opinion on the direction of technological progress?

Stanton: My motto, mantra, is that technological progress comes from doing things differently in an unpredictable way. The future is not an extrapolation of the past. You have to change how you do things. Some people don't realize that. I lecture at a lot of universities. I run into opposition from the nasty, noisy, negativists as I call them. You can't get here from there. It's impossible. An outstanding astronomer of the 19^{th} century, Simon Newcomb said, 'Man will never fly in an airplane.' Two months later, the Wright Brothers made their first flight. The year before Sputnik, Astronomer Royal Sir Richard van der Riet Woolley was quoted in *Time Magazine* as saying that 'space flight is utter bilge' and that 'nobody would every pay for it. What we need is better instruments for astronomy.' Mankind has a long history of underestimating change.



On the ELECTRONICS MANUFACTURING INDUSTRY and UFO RESEARCH:

Barry: Tell me about your experience here, at our industry event.

Stanton: This industry, well, I'm intrigued to be here for two reasons. First, it's proof that technological progress comes from doing things differently in an unpredictable way because whatever they're doing today is altogether different than the way it would have been done 20 years ago. Second, this is an international meeting. At least 49 countries are represented here. I am very worried about how we look to the aliens as a primitive society when our major activity is tribal warfare. We only killed 50 million people during WWII. That's pretty sad commentary, but here I see people from all over the world. They're exchanging ideas, talking to each other, being friendly, if you will, with each other instead of each one sticking to his own thing.

We all realize there's benefit from interchange. You may lose some sales, but in the bigger picture you're better off. I'm very pleased about it. I've got an eight-year-old great-grandson. I try to envision what the world is going to be like when he grows up.

Barry: It's a real treat to talk to you today. I really appreciate your time.

Stanton: My pleasure. I've enjoyed this conference. **PCB**

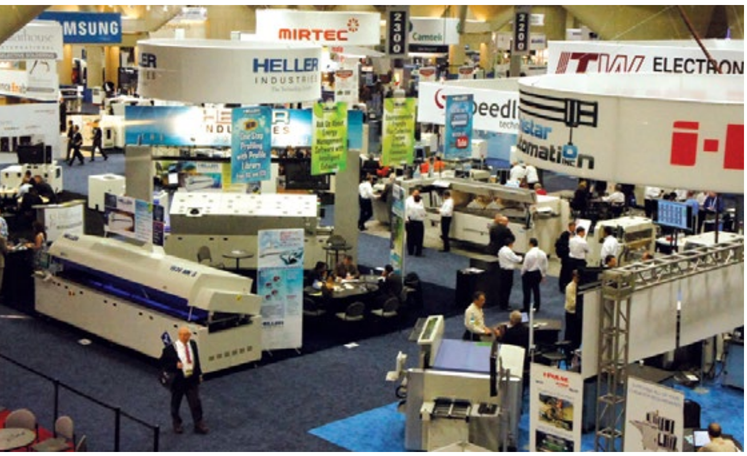
IPC APEX EXPO 2015: Allow for Serendipity

by Kelly Dack
I-CONNECT007 GUEST EDITOR

"If *plan A* doesn't work, stay cool! The alphabet has twenty-five more letters…"
—*Claire Cook, best-selling author and reinvention expert*

Andy Down!

At the start of the IPC APEX EXPO, my trade show coverage mentor and Managing Editor of The PCB Design Magazine and the PCBDesign007 newsletter, Andy Shaughnessy, was horribly under the weather and I was really concerned that he would not make it to the show from his home across the country in Georgia. But while he arrived eager to begin reporting and interviews, he was able to cover only a few events before being quarantined by his I-Connect007 team out of fear of being the first media organization to accidently record a lung being coughed up on-cam during an interview. Now, while Andy looked and sounded really sick, I don't think he was at all contagious. I spent a good deal of time before the show with him strategizing for some interviews and I even dined with him at a local sushi joint. And even as I write this, days later, I still feel great. Disclaimer: I do tend to spend a lot of time with Andy at the shows so I've built up plenty of immunity points. Andy asked if I'd submit my show perspective since his was shrouded in a haze of cough remedies. (I hope you are better my friend!)



Designer Forum

Once again, I was glad to have the opportunity to attend the Monday Designer's Forum event. This year's list of speakers included Carl Schattke, a PCB design engineer from Tesla Motors, who spoke on the subject of design for success.

PCB library expert Tom Hausherr, president of PCB Libraries Inc. discussed the IPC-7531C land pattern standard and generated quite a bit of audience engagement by presenting some new ideas for PCB component identification and marking.

IPC Master Trainer Rainer Taube, from Taube Electronic GmgH and FED Germany, spoke on component mounting issues and offered some recommendations in context of IPC-7070, for which he serves as committee co-chair.

Now, my usual plans for attending any designer event are clear: hear what industry icon Rick Hartley has to say. Rick speaks out of love and experience for every topic he chooses to discuss. At previous Designer Forum events I've heard him give kudos, and I've heard him be blunt. I've watched him yell at the top of his lungs while pounding on the lectern to make a point, and I've heard him explain the need to invest in yourself to an audience so mesmerized you could hear a pin drop. So I could only imagine that his talk this year on "success through control of cost and quality" would bring the house down. But as serendipity would have it, I got called out early for a previously arranged plant tour of Hallmark

Dieter Bergman Memorial Tribute

As planned, Wednesday evening I attended the memorial tribute to Dieter Bergman. I knew what to expect. I knew there would be food, drink, photos and good stories about the man Dieter. I expected tears of sadness at this gathering but felt joy for all of Dieter's friends and family when many of those who stepped up to tell a personal story about Dieter parlayed their experiences into tears of laughter from the audience. Many stories stood out about Dieter's bizarre foods affinity. As told, when travelling, Dieter made a point of sampling new foods. Some of which did a good job of upsetting his constitution. To soothe this, he and his meal-mates began enjoying a bit of ice cream after their meetings, which seem to help. Closing out an evening with ice cream quickly went from panacea to tradition for Dieter and many of his frequent companions.

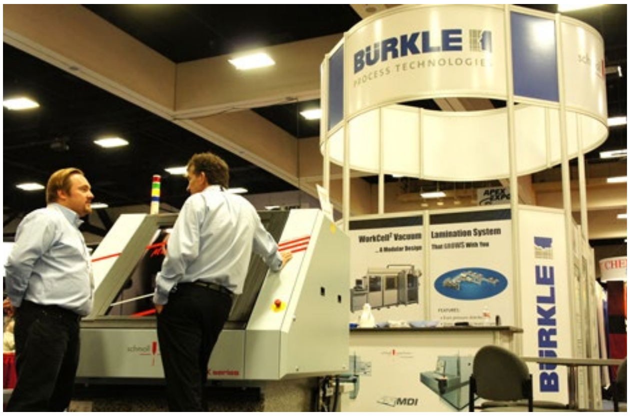
After the tribute ended, a group of thirty or so people decided to continue the ice cream tradition. My good friend and PCB designer, Jack Olson, and I, who had separately decided to venture into San Diego's Historic Gaslamp District for a visit, happened to be caught waiting for a light to change when the group caught up with us and extended an invite to join them to see how the ice cream tradition is done. So it was that some of Dieter's good friends who wanted to soothe the events of the past few months, the week and the evening, did just that—and the ice cream tradition continued.

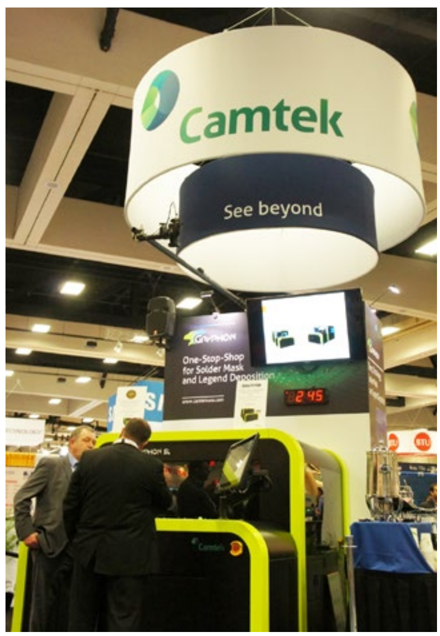
Hope to see you next year.

For Kelly Dack's complete show review, including notes on his evaluation and certification as a Certified Interconnect Trainer (CIT), and further details on Designer's Day Forum, be sure to read the March issue of The PCB Design Magazine. **PCB**

Dieter's last ice cream stand: From left: Bernard Kessler, Jo Ann Sotelo, Patty Goldman, Midge Ferrari, Gary Ferrari, (unidentified IPC member), Vern Solberg and Jack Olson.

2015 IPC APEX EXPO Show Review





2015 IPC APEX EXPO Show Review

SHOW REVIEW

2015 IPC APEX EXPO Show Review

SHOW REVIEW

2015 IPC APEX EXPO Show Review

Electronics Industry News
Market Highlights

[LED Industry to Face Challenging Market in 2015]
The market rise propelled enterprises to operate in full capacity, and even the enterprises that had been closed down resumed their capacity. But in the second half of 2014, the LED market plummeted and will very likely continue to worsen in 2015.

Automotive Industry to Boost M2M Services Market
"Increased awareness among vehicle owners about safety is expected to fuel the growth of the Global M2M Services Market during the forecast period," says Faisal Ghaus, Vice President of TechNavio.

Consumer Confidence on Tech Spending Remains High
Consumer sentiment toward technology spending and the overall economy shows strong readings for January after record highs in December, according to the latest data released today by the Consumer Electronics Association (CEA).

Smart City Technology Market to Top $27.5B Annually by 2023
"Cities are seeking partners and suppliers to collaborate on ambitious programs for sustainability, innovation in public services, and economic development that depend on significant technology investments," says Eric Woods, research director with Navigant Research.

DRAM Industry Up 8% in 4Q14
The average contract price in the fourth quarter was slightly above the prior quarter, driving up the growth of the DRAM market in 4Q14.

Silicon Wafer Shipments Achieve Record Levels in 2014
Worldwide silicon wafer area shipments increased 11% in 2014 when compared to 2013 area shipments, according to the SEMI Silicon Manufacturers Group (SMG) in its year-end analysis of the silicon wafer industry. However, worldwide silicon revenues increased by just 1% in 2014 compared to 2013.

Wearable Technology to Reach $22.7B in 2015
Wearable technology will be worth USD 22.7 billion in 2015 rising to USD 173.3 billion by 2020, but the long-term potential of the sector will make these numbers seem rather small.

Asia's Smartphone Growth to Slow in 2015
The relentless smartphone growth in the Asia-Pacific region is set to slow dramatically in 2015. Asia-Pacific's growth is set to drop from 43% in 2013 to 17% in 2014 and then to just 10% in 2015, largely driven as ever by China, according to market intelligence firm ABI Research.

Tablet Shipments Slow Down Dramatically
According to preliminary data, total tablet shipments reached 78.3 million units in Q4 2014, up 1% from 77.2 million in Q4 2013. Apple further consolidated its global market share, due to anticipated seasonal shipments reaching a 27% share of the tablet market.

Global MEMS Market Continues to See Increase in Demand
The increasing number of new applications in MEMS is one major trend upcoming in the market. Consumers are increasingly demanding smart devices such as fitness and health devices, smartwatches, and GPS-enabled devices, which have increased the demand for MEMS devices.

More Pesky Soldermask Problems: Plugged Via Leading to Skip Plating

by Michael Carano
OMG ELECTRONIC CHEMICALS

Introduction

Many factors are in play when it comes to preventing ink from remaining in vias. Two factors are presented here, and include phototool quality, the concept of D-min and D-max and optimal set-up of the developing step.

I am sure you have seen it, but may not have been sure of the root cause: solder not flowing in the vias and the lack of a plated solderable finish in the vias. Some of the vias have a final finish in them and others do not, and all of this happening on the same boards!

A closer examination yields solder mask ink remaining in the vias, resulting in what is essentially a plugged or partially plugged via. Some of the ink may also be present on the on the pads surrounding the vias (Figure 1).

This is not a pleasant situation and there is never an obvious fix, though you may be inclined to think so. After all, there is ink in the holes and it is not supposed to be there! The key is to not leave it there in the first place. However, it is not that simple.

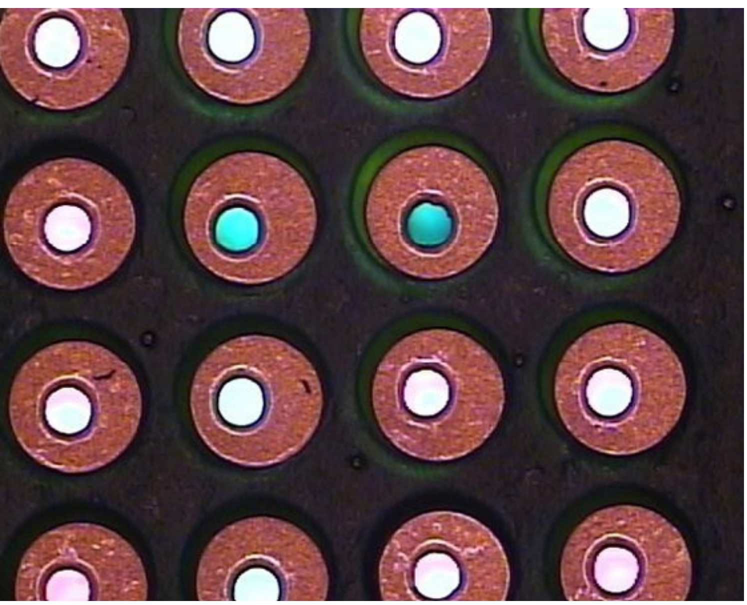


Figure 1: Green soldermask ink in via.

Getting to the Root Cause

It would be easy to just start pointing fingers either at the soldermask operation or the metallic etch resist process. Clearly something is preventing the deposition of the solderable finish into the via and on the pads.

There are several causes for the issue shown in Figure 1. As a troubleshooter, one must consider the following processes and properties:

- Viscosity and solids content of the LPI ink
- Excessive tack dry time and temperature
- Over exposure and/or under developing
- Phototool quality

Viscosity and solids content of the ink can be an issue with respect to ink remaining in the holes (especially smaller diameter vias). When adjusting the viscosity of the ink, ensure that a sufficient amount of solvent is added to the ink. Under-adding of the solvent will increase the solids content and adversely affect the viscosity. If the material is too viscous, there will be excess ink in the vias, therefore increasing the difficulty of complete removal. Mask suppliers will provide a thinner to adjust the ink viscosity. Interestingly, there is a greater chance that holes can remain plugged with double-sided screen printing as opposed to either curtain coating or spray coating of the ink.

The principal of double-sided screen printing is embodied in the functional aspect of the screen printing equipment that allows for the coating of both sides of the printed circuit board simultaneously (Figure 2). The screens are fixed at the same distance from both sides of the board. There are also squeegees in the same

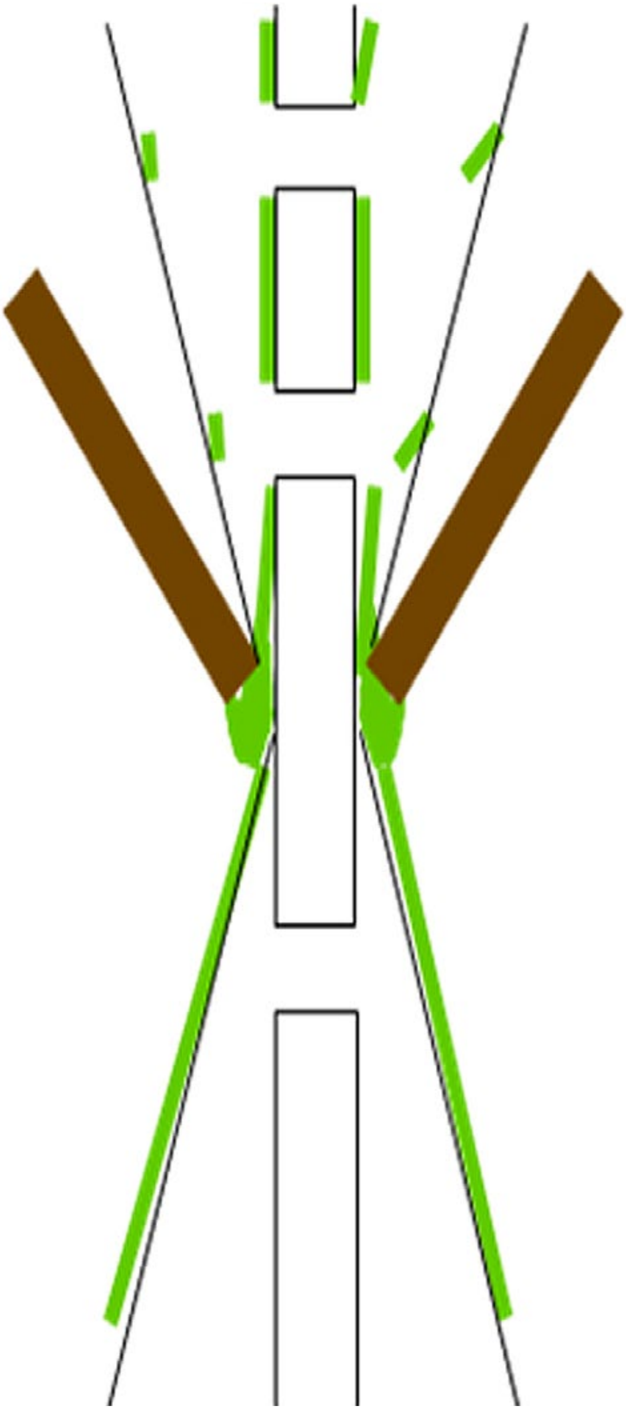


Figure 2: Double-sided screen printing. (source: Lackwerke Peters GmbH)

relative position on the opposite sides of the PCB. Pressure that is applied to the squeegees from both sides is identical. After screen printing, there will be more ink in the vias than is noted with either spray or curtain coating of soldermasks.

While additional ink in the holes is a given with double-sided screen coating technology, excessive tack dry time and temperature is of equal concern. By over-drying, the ink has a much greater chance of solidifying in the via, making the ink plug more difficult to develop away.

Subsequently, that brings us to the issue of phototool quality and the exposure/developing process steps. The phototool has two particular features that should be evident. There is the clear area that allows UV light to pass through and the opaque or darkened areas designed to prevent the light from passing. Where the light is able to pass, the ink will undergo polymerization. And that's where the concept of D min and D max show up: the optical density of the clear and opaque areas of the phototool.

The reader should also familiarize herself with the term densitometer. Proper mastery of this instrument will help to ensure optimum quality of the phototool. D-min is a measure of the tool to transmit light. The lower the number, the greater the transmission. And that is what the engineer wants, maximum transmission of the UV through clear area of the tool. D-max, on the other hand, is a measure of image area on the tool and its ability to block the UV light. The densitometer, thus, is an instrument that is used to measure and track the D-min and D-max attributes of the phototool. This concept is introduced here for one reason; as the D-max decreases (or is not high enough from the beginning) there is a greater chance for UV light to penetrate the tool and cause partial or complete exposure of the ink. This would then cause difficulty when trying to develop out the ink from the holes. There is also the chance that some of the ink may be exposed on the pads, which can then lead to non-conformance. The best advice is to use the densitometer to monitor the D-min and D-max of the tool. After repeated exposures, the D-min will increase and the D-max will decrease. As a rule of thumb, a newly produced phototool should have a D-min between 0.08–0.11 and a D-max of 4.0 or more. When the D-min increases above 0.20 and the D-max decreases to a measured value below 3.8, it is time to produce and use a new phototool.

Even with the proper exposure technique and high quality phototool, LPI ink may still remain in the vias due to poor developing. Even if one assumes that the ink in the via is not partially exposed (due to low D-max) or over dry (tack dry issues), improper control of the developing operation reduces the effectiveness in removing ink from the vias. With respect to developing, the greatest difficulty is encountered in removing the unexposed ink from small diameter vias. The prerequisites for good developing then are:

- Sufficient amount of spray nozzles in the developer chamber
- Combination of different spraying angles and spray patterns
- Implementation of low-pressure, high-volume nozzles
- Implementation of permanent wetting of squeeze rollers
- Use of high performance blowers (needed for dry holes)
- Maintenance of sodium carbonate levels in developer between 0.9–1.1%, by weight

If one follows these key items, the developing quality will prove to be excellent. **PCB**

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

Making High-quality Fiber-based Electronic Devices

Scientists have known how to draw thin fibers from bulk materials for decades. But a new approach to that old method, developed by researchers at MIT, could lead to a whole new way of making high-quality fiber-based electronic devices.

The idea grew out of a long-term research effort to develop multifunctional fibers that incorporate different materials into a single long functional strand. Until now, those long strands could only be created by arranging the materials in a large block or cylinder called a preform, which is then heated and stretched to create a thin fiber that is drastically smaller in diameter, but retains the same composition.

Now, for the first time, fibers created through this method can have a composition that's completely different from that of the starting materials—an advance that lead researcher Yoel Fink refers to as a kind of "alchemy," turning inexpensive and abundant materials into high-value ones. The new findings are described in a paper in the journal Nature Communications co-authored by graduate student Chong Hou, and six others at MIT and in Singapore.

The fibers are made from aluminum metal and silica glass, abundant low cost materials, which are commonly used to make windows and window frames. The aluminum metal and silica glass react chemically as they are heated and drawn, producing a fiber with a core of pure, crystalline silicon—the raw material of computer chips and solar cells—and a coating of silica.

Best Practices 101, Part 5: Process Capability

by Steve Williams
STEVE WILLIAMS CONSULTING LLC

Early in my career, a wise old mentor told me, "Steve, never argue about what can be measured." As an engineer by trade and German by lineage, he knew a little about precision craftsmanship. This advice has stuck with me, and in the quest for continuous improvement it has translated into "How can we get better if we don't know where we are now?" followed by "How can we know where we are now without metrics?"

Process Capability

I will try to follow my KISS philosophy and stay away from all the scary math as much as possible, so let's begin by reviewing the fundamentals of statistical process control (SPC). It is important to note at this point that not every process is a good candidate for statistical control, and that in these instances alternate process control methods may be required. The laws of physics dictate that although every single process has variation, once a process is stable, that variation follows a repeatable pattern that is called a *normal distribution*. That means that only some of the product (any process output) will be exactly the same as the process average (mean). It also means that the rest of the product will either be less or greater than the average, and will occur in decreasing frequency the further away from the mean the data stray. If you were to draw this product data set in graphical form, it would take the shape of a bell, which is why a normal distribution is also called a *bell-shaped curve*. Another thing that is known about a normal distribution is that the relationship of the product that falls on either side of the mean is predictable. In other words, the data can be divided into groups based on the distance (deviation) from the mean. The term *standard deviation* is used to describe these groups.

Every product has an optimum value, and because every process has variation, it also has a tolerance. This is defined as specification limits, with both an upper and lower spec limit (USL, LSL) surrounding the optimum value. Simply stated, when a product or process is outside of either of these spec limits, bad product is produced. How well the process variation is centered and contained within these spec limits is called *process capability*. The relationship of this

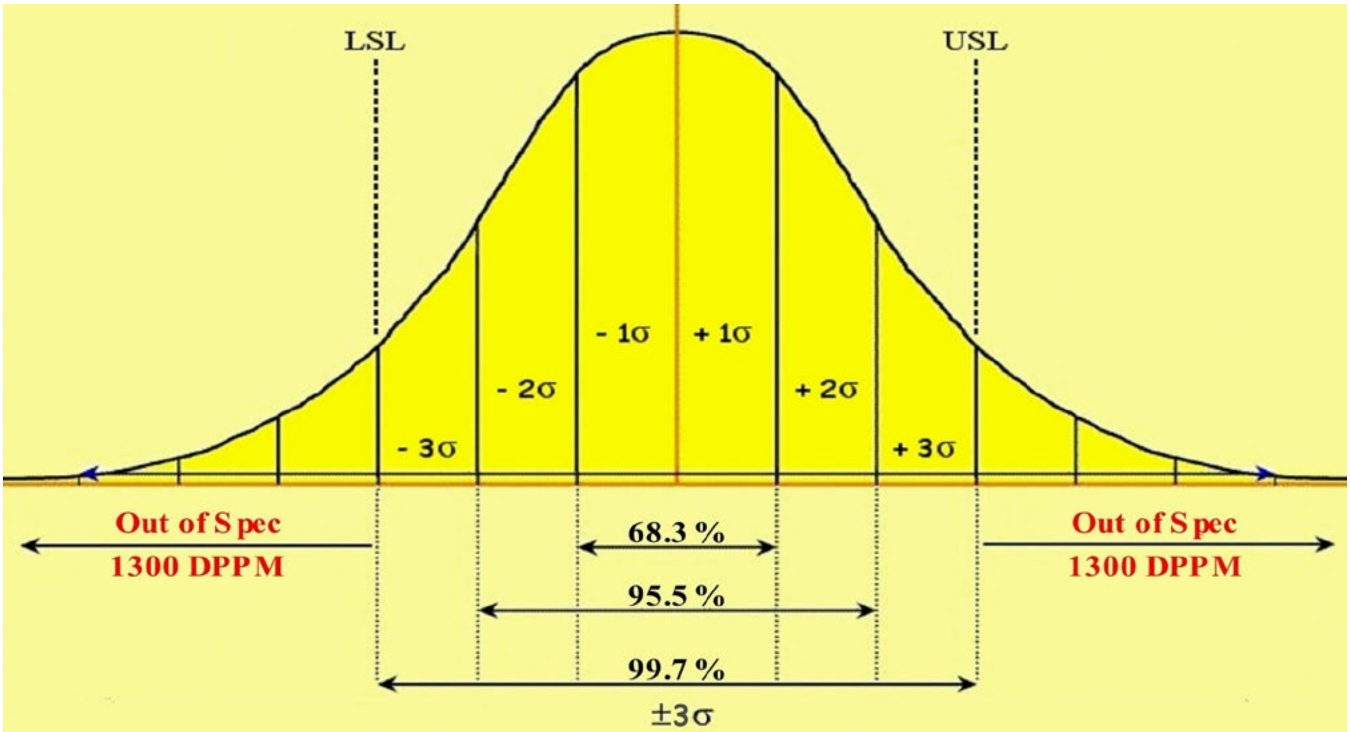


Figure 1: A normal distribution, where 99.7% of variation falls within +/– three standard deviations, or sigma levels.

variation to the mean and spec limits is the process capability, or Cpk. The less variation in a process, and the closer the variation is to the mean, the higher the Cpk number. With all the statistical tools available, the formula is not important for this purpose, but what is important is recognizing what this number means. It is generally accepted that a Cpk of less than 1.33 would indicate a process that is not capable of consistently meeting customer requirements, and a Cpk of 2.0 would represent a six sigma level. The sigma level represents how many standard deviations, or sigmas, it takes to reach the spec limits on either side of the mean. In other words, in a three sigma process it takes three sigmas to reach the LSL and three sigmas to reach the USL.

Sigma Levels

The sigma level is a difficult concept to understand during the early stages of process improvement, so I will try to simplify this as much as possible. When a process is referred to in sigma terms, it is stating how many sigmas (standard deviations) it takes to reach the specification limits from the mean. Statistical rules state that the amount of variation that falls within each group, or sigma level, is repeatable and can be quantified. It is important to remember that these rules are constant regardless of what sigma level a process is operating under.

Most organizations have not achieved a 99% yield, much less a three-sigma level. As Figure 1 shows, in a normal distribution, 99.7% of the variation will fall within +/– three standard deviations, or sigma levels. While that may appear to be a very good yield on the surface, this translates into 2700 DPPM that will fall outside of the specification limits. The areas outside of the spec limits are called the process *tails,* and again referring to Figure 1, these tails fall outside the spec limits and represent defective product. As we saw earlier in this chapter, a three sigma process results in an awful lot of defective product.

Now let's look at a six sigma process, where it takes six standard deviations, or sigmas, to reach each spec limit. Again, statistical rules state that 99.9997% of the variation will fall

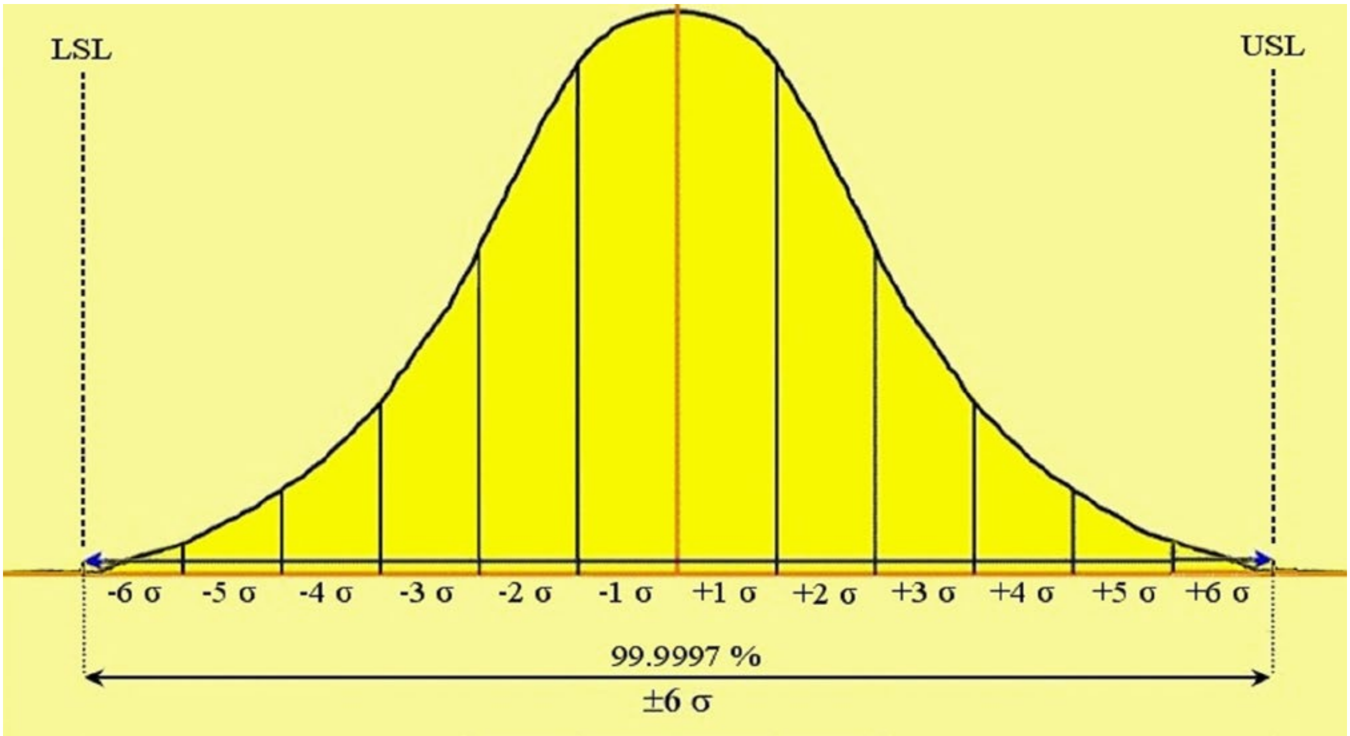


Figure 2: Tails are contained within the spec limits, assuring that virtually no product will be produced out of specifications.

within +/– six standard deviations, or six sigma levels. As Figure 2 indicates, the tails are contained within the spec limits, assuring that virtually no product will be produced out of specifications (3.4 DPPM, or two defects outside each spec limit).

It's OK To Take Baby Steps

The key takeaway here is that improvement should be taken in steps; don't expect to jump from three to six sigma overnight. Sigma levels range from one to six, and legitimate process improvement generally follows a natural progression from the current level up through this range. The first step is to make sure you are at a true three sigma level; most organizations are surprised to learn that they have a lot of work to do to reach this plateau. The next step is to make incremental improvements to begin moving up the sigma ladder. Quantum improvement can be realized by moving up just a single sigma level; remember that the key to success in improvement is to hit singles, not home runs!

Given the zero defect goal discussed here, and the general perception that six sigma levels are unachievable, I thought it appropriate to close with the following quote from the chief engineer of Toyota's first Lexus; a man called the "Michael Jordan of chief engineers":

"Even if the target seems so high as to be unachievable at first glance, if you explain the necessity to all the people involved and insist upon it, everyone will become enthusiastic in the spirit of challenge, will work together, and achieve it." –Ichiro Suzuki, Toyota Motor Corporation **PCB**

Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

PCB007 Supplier/New Product News Highlights

Ventec USA Expands Sales Force

Ventec USA, a member of the Ventec International Group, leading manufacturer of high-quality, high-performance copper clad laminates and prepregs, is delighted to announce the appointment of two sales professionals to further augment its presence in the North American market.

Isola Unveils New Technical Education Series

Isola Group S.à r.l., a market leader in copper-clad laminates and dielectric prepreg materials used to fabricate advanced multilayer PCBs, today announced the launch of a new Technical Education Series (TES) to address the increasingly important role of laminate materials in the overall process of system-level design.

Wurth Elektronik Invests in Orbotech's Direct Imaging

Orbotech announced today that German PCB manufacturer Würth Elektronik has selected Orbotech as their vendor-of-choice for direct imaging (DI) technology with the purchase of the latest Nuvogo 800 DI system.

Orbotech's PCB Equipment Sales Down in Q4

Commenting on the results, CEO Asher Levy said: "2014 was a turning point for Orbotech, reflecting our uncompromising commitment to deliver on the growth strategy that we had marked out in 2013. We are pleased, as a result, to report record annual revenues, as well as solid results for the fourth quarter, concluding what has been a strong and transformational year for the company."

Insulectro Purchases New Warehouse in Minneapolis, MN

Insulectro President and CEO Tim Redfern commented, "We are pleased to expand our presence in the Midwest electronics markets, especially near the Twin Cities. With so much PCB and printed electronics activity in the greater Minneapolis market it makes sense for us to continue our strategy of acquiring property. We've just outgrown our current location of 12,000 square-feet in Golden Valley, MN."

Uyemura Taps International Process Technologies to Expand Footprint

International Process Technologies will represent Uyemura throughout Minnesota, Wisconsin and the Upper Peninsula of Michigan.

LPKF Continues to Build on LDS Business in China

LPKF has received an order worth 2.5 million from a Chinese electronic manufacturer for laser direct structuring (LDS) systems. This is the first phase of a large-scale order LPKF was expecting in the fourth quarter of 2014, but which the client postponed.

Prototron Focuses on New Product Development

"Because we are so focused on new product development, we find DesignCon a very productive show every year. It puts us face to face with all of the right people, designers and new product engineers so that we always walk away with some very interesting leads and opportunities," commented Ryder.

Camtek's Q4 Revenue Drops but FY 2014 Remains Positive

Rafi Amit, Camtek's Chairman and CEO, commented, "I see 2014 as the year in which we put all the pieces in place and began executing on our strategy for accelerated growth in 2015. As we recently reported, we have started commercially marketing the Gryphon, our 3D Functional InkJet Technology product and received our first conditional purchase order for this product."

Rogers Expands Solutions; Completes Acquisition of Arlon

Bruce D. Hoechner, president and CEO commented: "We are very pleased to formally welcome Arlon's employees to the Rogers team. This acquisition provides Rogers with unique growth and diversification opportunities for two of our strategic businesses and aligns well with both our long-term strategy to grow through selective acquisitions, as well as organically. We are excited to begin our work with Arlon's team to expand our solutions and better serve our customers around the world."

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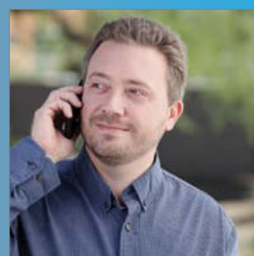

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Optical Interconnects

by Karl Dietz
KARL DIETZ CONSULTING LLC

When we hear of optical interconnects or optical signal transmission, we think of the long-distance signal transmission through glass fibers, the conversion of ocean floor cables to glass fibers, and the establishment of glass fiber transmission lines between cities in the late 1990s, followed by intra-city glass fiber lines and glass fiber networks that connect buildings[1].

Then, chip-to-chip optical interconnects were explored, and when data rate transmissions in backplanes pushed beyond 10Gbits/sec, the limitations of conversional signal transmission through copper over 500 mm line length, and beyond, became apparent, especially with conventional, affordable dielectric material platforms. Signal attenuation and signal shape distortion became unavoidable, even with differential signaling and back-drilling of metalized through-holes. Optical backplanes hold the promise of avoiding these problems. There are practically no transmission losses and no electromagnetic interferences, and the capacity to transmit an enormous amount of data is unsurpassed. Optical transmission can be through optical fibers, waveguides, or through air, or a combination thereof. However, the cost of the optoelectronic components and the cost of precision mounting has been a major hurdle to moving to optical backplanes.

Lucent looked at the development of optical backplanes in the early 2000s, but financial problems interfered. Of particular interest were

2015 Programs

April 29–30
IMPACT 2015: IPC ON CAPITOL HILL
Washington, DC, USA

May 13–14
IPC Technical Education
Fort Worth, TX, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

June 9
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Fort Lee, NJ, USA

June 9–10
IPC Technical Education
Chicago, IL, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

June 10
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Des Plaines, IL, USA

June 12
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Milpitas, CA, USA (San Jose area)

September 27–October 1
IPC Fall Standards Development Committee Meetings
Rosemont, IL, USA
Co-located with SMTA International

September 28
IPC EMS Management Meeting
Rosemont, IL, USA

October 13
IPC Conference on Government Regulation
Essen, Germany
Discussion with international experts on regulatory issues

October 13–15
IPC Europe Forum: Innovation for Reliability
Essen, Germany
Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27
IPC Technical Education
Minneapolis, MN, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

October 28–29
IPC Flexible Circuits-HDI Conference
Minneapolis, MN, USA
Presentations will address Flex and HDI challenges in methodology, materials, and technology.

November 2–6
IPC EMS Program Management Training and Certification
Chicago, IL, USA

November 4
PCB Carolina 2015
Raleigh, NC, USA

December 2–3
IPC Technical Education
Raleigh, NC, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting

December 2–4
International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)
Shenzhen, China

Questions? Contact IPC registration staff at registration@ipc.org or +1 847-597-2861

OPTICAL INTERCONNECTS *continues*

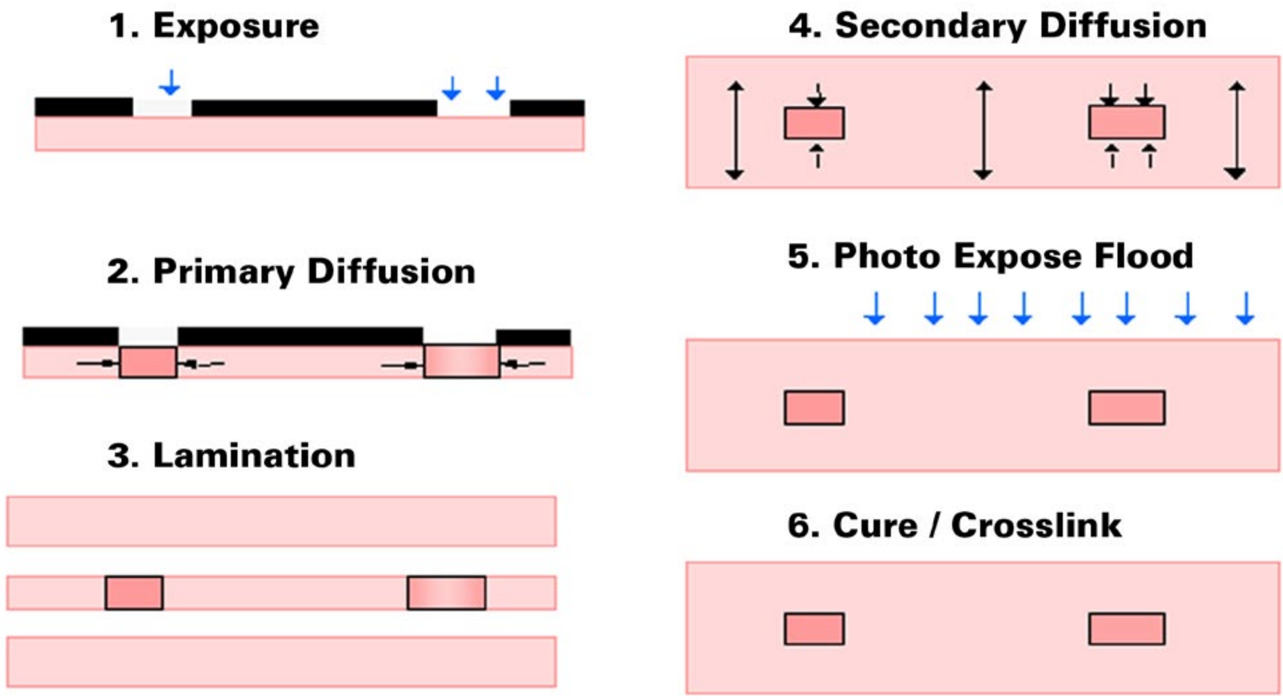

Figure 1: Dry process photolithography for waveguide formation.

organic waveguides based on dry film photoresist technology such as DuPont's Polyguide™. UV exposure changes the optical properties of the waveguide from the surrounding unexposed material. The material base for such waveguides was acrylate chemistry, which limited the transmission distances because of the lossy material and was limited to a transmission mode called multimode. The use of lower-loss photosensitive fluorinated polyimides was technically feasible but costly and raised concerns about the toxicity of the chemicals.

Waveguides come in a variety of material constructions: organics, glass, silica, silicon, etc. The properties that are important to the performance of waveguides include:

- Intrinsic absorption loss
- Low optical scattering loss
- Low waveguide fabrication loss
- High thermal stability
- Environmental stability
- Precise control of refractive index
- Low birefringence
- Mechanical toughness

Before waveguides were considered for optoelectronic integration into PWBs, notably backplanes, they could be found in wafer-scale packaging. A polymer cladding is typically applied onto either silica or silicon wafer supports using spin coating technology. Good coating uniformity and precision is achieved with this process over the surface of the wafer. Then a guide polymer of a higher refractive index than the cladding is spun on and patterned either by virtue of its own photosensitivity or with a layer of photoresist, sometimes over a metal mask. The thicknesses of the waveguide layer are in the range of 5–60 microns. The waveguide pattern is then formed by etch-back, usually by plasma, but sometimes by solvent. Then a final layer of cladding is spun on and the wafer is complete. It is diced, connected to fibers, mounted on a support such as glass or ceramic, perhaps on a heater or thermoelectric cooler, placed in a package and electrically connected.

There are several processes to form polymeric waveguides. One of them is a photoimaging, all-dry process (Figure 1). Waveguide forming films with mobile monomers and polymer binders along with initiators and other constituents are pre-coated on a temporary polyester substrate carrier with a polyester protective sheet. The film is exposed, causing photopolymerization in the exposed areas that will become the wave paths. After exposure, monomers diffuse from the monomer-rich adjacent areas into the monomer-depleted exposed areas, creating features with a higher refractive index than their surroundings. The exposed film is then laminated between two unexposed films from which more monomers diffuse into the exposed sections. Subsequent flood photoexposure and curing form the mechanically and thermally stable structure of the waveguide and its cladding, without destroying the refractive index difference between guide and cladding.

Because of the high optical attenuation of polymer-based waveguides, there has been a continued interest in lower-loss glass-based waveguides. The work described in Reference 2 aims at the formation of electrical-optical circuit boards, using photolithographic and ion exchange processes to form graded-index multimode waveguides in thin glass, which is embedded in the circuit board. The thin glass was a commercially available product from Schott. The glass is first cleaned, then double-sided coated with an aluminum diffusion mask. Next comes the double sided coating of photoresist, mask alignment, UV exposure and development. The diffusion mask is then etched and waveguides are then grown in the glass by ion exchange, followed by removal of the diffusion mask. The work was done by a consortium, including research institutes (e.g., Fraunhofer IZM), universities, a circuit board manufacturer (Wuerth Elektronik), and suppliers to the industry such as Siemens AG.

The following communications document continued interest and work on optical backplanes:

• In a news release from HP Lab in EE Times (February 6, 2012), HP describes a 30 GByte/s optical backplane it created as a tech demo for its ProCurve 9200 switch. The backplane was built from a hollow metal waveguide bundling 12 10 Gbyte/s optical channels.

• Posted in EE Times (October 5, 2012), Altera explains the move from copper to optical backplanes. The 56Gb/s backplane technology makes this transition necessary. A standard for this new platform is expected to be developed with two to three years.

• In their presentation "Optical Backplanes—Fantasy or Reality?" Beth Murphy and Scott Schaeffer of Tyco/Electronics/AMP give a detailed overview of optical backplane applications such as inter-rack, intra-rack, and inter-device backplanes. They see some extension of copper backplane technology on the basis of lower loss laminates, but see plated through-holes as a major performance issue.

• iNEMI offered a "Roadmap for Optical Backplanes—A Copper vs. Opto Business Analysis" presented by Jack Fisher at the LEOS HSD Workshop, May 14–17, 2006, Santa Fe, New Mexico.

So, it appears that after a hiatus in the mid 2000s there is again a renewed interest in optical backplanes, a development worth following. **PCB**

References

1. "Low-Cost Optical Interconnect Expected for GHz Boards," by Masahiro Katoh and Chikashi Horikiri, February 2002 Issue, Nikkei Electronics Asia.

2. "Thin Glass Based Electro-Optical Circuit Boards (EOCB) Using Ion-Exchange Technology for Graded-Index Multimode Waveguides," Henning Schroeder et al., Proceedings, pg. 268, 2008 Electronic Component and Technology Conference.

Karl Dietz is president of Karl Dietz Consulting LLC. He offers consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, click here. Dietz may also be reached by phone at (001) 919-870-6230.

Highlights from PCB007 this Month

1 California Congressman Mike Honda Discusses American Manufacturing

Barry Matties, publisher of I-Connect007, sat down with Congressman Honda, who represents District 17 in the Silicon Valley, to talk about American manufacturing, infrastructure, education and some of the current thinking in America. According to Honda, "The policies we pass and the things we do in D.C. that negatively impact our economy...a lot of those guys who don't support some of the positive things we want to see happen don't really understand that it impacts their districts, their social services, health and business."

2 DSG Invests in the Future

Mauro Dallora, COO of Dongguan Somacis Graphic PCB Co. Ltd (DSG) shares how they have increased revenue and their plans to double it.

3 MacDermid's Cullen Reflects on 20 Years in China

Recently, while in Shenzhen, China, Barry Matties had the chance to catch up with Don Cullen, the global marketing director at MacDermid Electronics Solutions. They sat down to discuss the many changes he's seen in China since his first visit there nearly 20 years ago, and the country's future.

4 Viasystems Reports Solid Q4 2014 Results

"The settlement of our business interruption insurance claim certainly helped our reported profit for the period," noted David M. Sindelar, chief executive officer of Viasystems, "but even without that favorable impact, we had a solid quarter, growing net sales both sequentially and year-over-year."

5 N.A. PCB Business Growth Flat in 2014

"PCB business in North America was virtually flat in 2014 compared to the previous year," said IPC's Sharon Starr. "Sales ended the year less than one percentage point below 2013, while orders finished the year just 0.6% above 2013. Strong orders in the fourth quarter have kept the book-to-bill ratio solidly in positive territory, which bodes well for sales growth in 2015."

6 China Outlook: An Interview with Hamed El-Abd, Lionel Fullwood, and Gene Weiner of WKK

Barry Matties spoke with WKK's Hamed El-Abd, Lionel Fullwood, and Gene Weiner on their outlook on PCB manufacturing in China, as well as on what it takes to stay competitive in this market.

7 Exception PCB Names Martin Managing Director

Frederick Martin has been appointed as managing director for Exception PCB Solutions and brings a wealth of experience. Frederick will join Clive Wall and Rob Buswell in the Senior Management Team. The senior management are a highly experienced and results driven team that has the proven capability to implement Fastprints' European strategy and leverage the business's undoubted potential.

8 2015 EIPC Winter Conference, Munich: Day 1 Review

Ninety delegates, eleven countries represented and a thought-provoking two-day programme on themes of reliability in PCB fabrication and assembly, copper cleaning and advanced material solutions, advanced imaging and soldermask, and how to make PCBs smart and ready for Industry 4.0. Add the further attractions of a keynote by Walt Custer and the chance to visit a military aircraft assembly plant: the formula for another highly successful EIPC Conference—this time close to Munich Airport.

9 Schweizer Electronic Concludes FY2014 with Sales Growth

Dr. Maren Schweizer, CEO of Schweizer Electronic AG comments: "We proceeded very well in 2014 on operational as well as strategic levels. We increased turnover and earnings, and our order book is well stocked. Thanks to the continuously high demand our order backlog increased again in 2014, amounting to 119.2 million euro against 114.2 million euro the year before."

10 PCi Upgrades Imaging Department with New Equipment

Rigid-flex circuit board manufacturer, Printed Circuits Inc. has recently installed a Maskless Lithography printer and an Orbotech Paragon 9800 laser-direct imager at their facility based in Minneapolis, Minnesota.

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

FPD China 2015
Shanghai, China
March 17–19, 2015

Puget Sound Advanced SMT Chapter Tutorial Program
March 17, 2015
Puget Sound, Oregon, USA

Process Optimization and Defect Elimination for PCB Assembly
Webinar: March 18 & 25, 2015

Shining a Light on LED Technology
Webinar: March 19, 2015

Dallas Expo & Tech Forum
March 24, 2015
Plano, Texas, USA

Houston Expo & Tech Forum
March 26, 2015
Stafford, Texas, USA

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Coming Soon to *The PCB Magazine:*

April:
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May:
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Flex