THE pcb design MAGAZINE

May 2015

an I·Connect007 publication

The Do's and Don'ts of Signal Routing for Controlled Impedance
p.18

Impedance Control, Revisited
p.24

CONTROLLED IMPEDANCE

Controlled Impedance Design

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This Issue: CONTROLLED IMPEDANCE

FEATURED CONTENT

Controlled impedance PCBs are becoming more common now, especially in high-speed applications. Designing these boards can be particularly challenging. This month our expert contributors Barry Olney of In-Circuit Design, Martyn Gaudion of Polar Instruments, and Mark Thompson of Prototron Circuits focus on the ins and outs of controlled impedance design.

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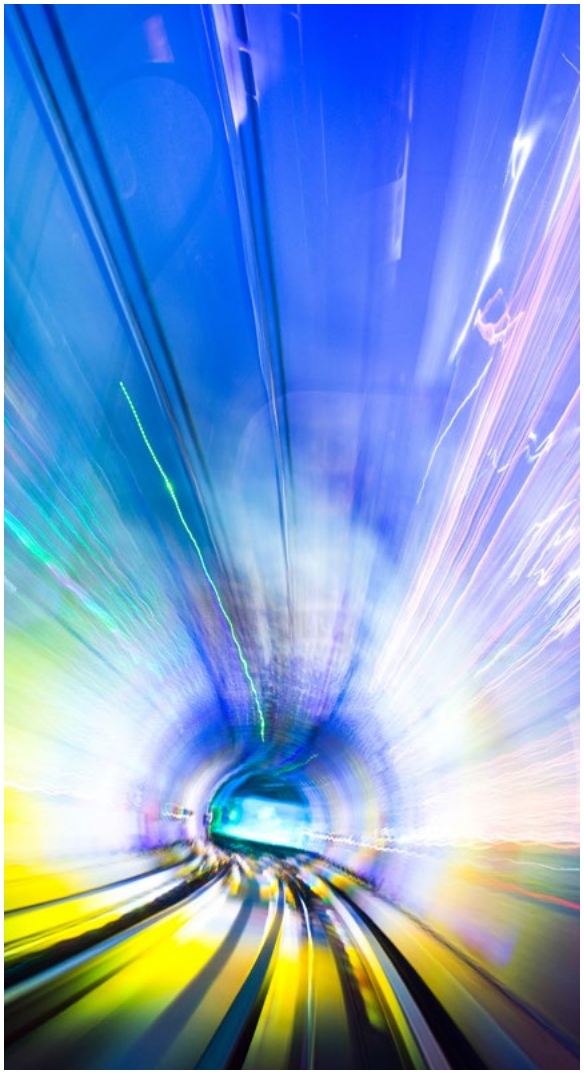
by Barry Olney



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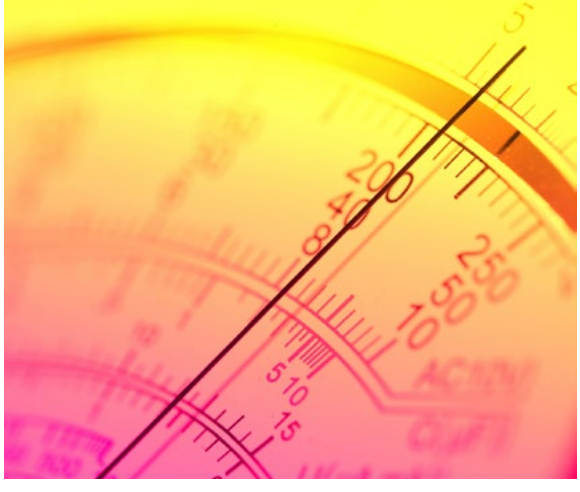

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Df @ 10 GHz	0.0028 - 0.0036	0.0028, 0.0031 & 0.0034	0.0031*	0.0030*	0.0017
CTE Z-axis (50 to 260°C)	2.90%	2.80%	2.80%	2.90%	2.90%
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Halogen free	No	No	No	Yes	No
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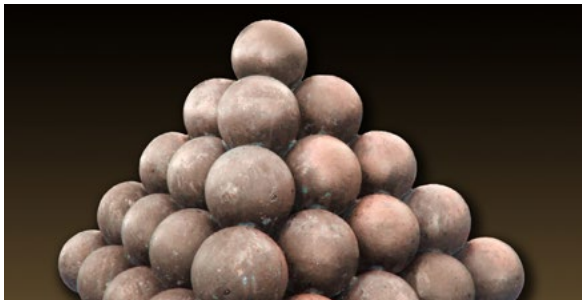

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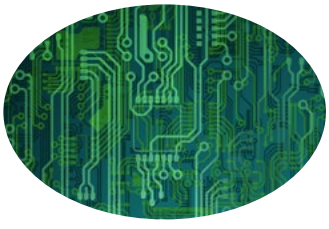

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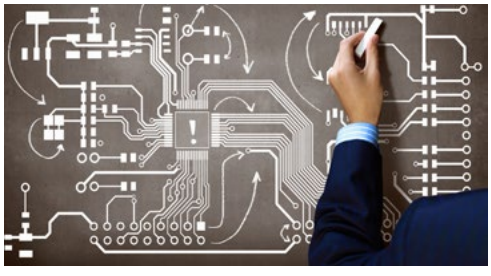

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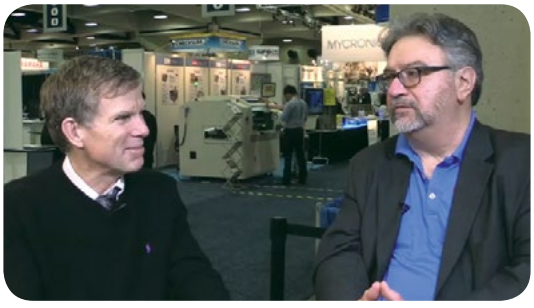

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The Readers Speak

by Andy Shaughnessy
I-CONNECT007

I wish I could read minds. If I could, I'd know exactly what sort of problems you all face when you're designing PCBs, what sort of technology you're working with, and what sort of trends you're seeing in PCB design and PCB manufacturing.

But since I'm not clairvoyant, I have to resort to other means to find out about our readers' trials and tribulations. This is where our reader surveys come in. The survey is one of the best ways for us to find out about you and your job, which helps us to be certain that we're providing you the most relevant content possible.

Best of all, surveys give the reader a voice. What's on your mind? We really want to know.

Recently, we sent out a survey with a handful of questions; we've found that surveys with too many questions don't get answered. One question was, "Does supply chain management affect your job?"

The answers were surprising. Almost 2/3 of you said no, the supply chain doesn't affect your job in any meaningful way. But a third of you said the exact opposite: The supply chain impacts your job directly, and for some of you, it's a big problem.

A very vocal minority left us a variety of great comments regarding their supply chain challenges. Here is a sample of the comments for that question:

- New parts availability and older parts going obsolete.
- Availability of parts.
- Component/part selection.
- The part selection process at the front end of the design.
- Component availability and end of life. Medical products could have a 15-year life.
- Replacing old parts, verifying parts are active and available.
- Cost factor and similar vendor capability for second source.
- Design updates after the board is complete due to part limitations.
- Having to correct layout due to changed components.
- Orders for parts affected by proposed ECOs have to be factored in, as procurement has outstanding orders for not only parts affected, but parts that may be affected by the ECO.
- Didn't used to, but as we go to higher frequencies into the millimeter wave range (like 60-86 GHz), the material choices, component choices, and fabricator choices decrease. We are having to source and stock material ourselves.
- Company changes CM from proto to production. Sloppy production at best.
- Cannot predict board and component suppliers in certain projects.
- Late changes to component selection due to too long delivery.
- Too much bureaucracy! Too many hands in the pie! Singular POC personnel for many tasks is WAY TOO MUCH!

You designers in the minority are serious about this. But why did the majority of respondents say that the supply chain had no effect on their job? I imagine it depends upon your employer; do some OEMs have a foolproof system for managing the supply chain?

I can't help wondering why there's such a huge dichotomy here, with most respondents saying, "No problems with the supply chain here," while a third of you are having a tough time ensuring that the necessary components, parts, and materials are available for your designs. What do you think—is the supply chain a problem for you? Let me know what you think.

We also asked, "When designing a PCB, what are your greatest challenges?" Here are some of the best comments for that question:

- Getting correct and complete information from the engineers.

- Engineering, and getting the circuit completed and final on a timely basis.
- Engineers.
- Getting a complete schematic/rules.
- Receiving PCB requirements when starting a design.
- Bugs in the software.
- The bad design tool.
- The density and small pitch of the BGA components.
- Keeping the hole-to-copper clearance, especially when routing diff pairs within a BGA area.
- Getting out of large BGAs without the use of HDI.
- Maximizing the most out of the available space.
- Getting it all to fit and be routable and DFM in the board size.
- Board size vs, density.
- Space for components and space for tracking.
- To fit everything in the board space.
- Fitting everything into small areas and keeping costs low.
- Fitting small component packages elegantly on large transmission lines.
- Meeting deadlines.
- Time. (3x)
- Time to market.
- Meeting schedules.
- Stackup design.
- Impedance control.
- Signal integrity.
- Getting paid.
- Customer stupidity.

We see some definite trends here. Communication with engineers seems to be a constant complaint among designers, and that's reflected here. Do any of you have a great working relationship with your engineers? It may be just an interdisciplinary difference in working styles, but there's certainly a disconnect between designers and engineers.

The lack of time and shrinking board space are other repeat answers. I'm not sure that there's a fix for these problems; time-to-market and board space are always decreasing. Then there's the bad EDA tool, another constant refrain from designers. And you have to love the last answer, "customer stupidity."

Finally, we asked, "What is the most important thing you have learned on the job in the past year?" Here are some of the more interesting comments:

- To reduce my hourly rate by a factor of 3 and multiply my reported work hours by a factor of 5.
- That I could have made a lot more money with a business/management degree!
- Communication is critical no matter where you are located.
- Take more time to evaluate parallel designs done by outside vendors before setting design schedule.
- Workarounds for lousy PCB software.
- There are many "experts" on CAD layout who want to help me.
- Not to design on the edge of technology.
- Good time estimation for different kind of projects.
- More people involved means more delays and more chaos.
- That all PCB vendors are not honest.
- Allegro PCB Editor is a real mother to learn how to use.
- Allow more time for the mechanical designer to finished his part of the design.
- How to handle DDR3 implementation.
- Cost is not king.
- Breaking out .5 mm BGAs.
- Nothing.

As always, we appreciate the input from everyone who responded to this survey. You can be sure that we'll be pinging you again in the future. These surveys help us stay informed about the challenges you face, and they also provide you with a soapbox. If you want to make your voice heard, answer one of our surveys. We just might post your comments. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.

Controlled Impedance Design

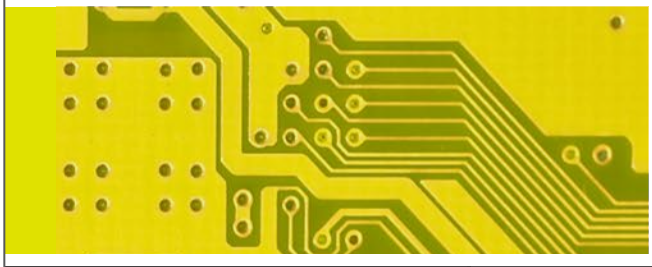
by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Controlled impedance—it's all about transmission lines. For perfect transfer of energy, the impedance of the driver must match the transmission line. A good transmission line is one that has constant impedance along the entire length of the line, so that there are no mismatches resulting in reflections. But unfortunately, drivers do not have the exact impedance to match the line (typically 10–35 ohms) so terminations are used to balance the impedance, match the line and minimize reflections.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance.

Impedance matching slows down the rise and fall times, reduces the ringing (over/undershoot) of clock drivers and enhances the signal quality of a high-speed design. The ringing is dramatically reduced by adding a series terminator as in Figure 1. From this, we can see that the impedance has to be matched, but to what value?

MEC FROM UIC



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CONTROLLED IMPEDANCE DESIGN *continues*

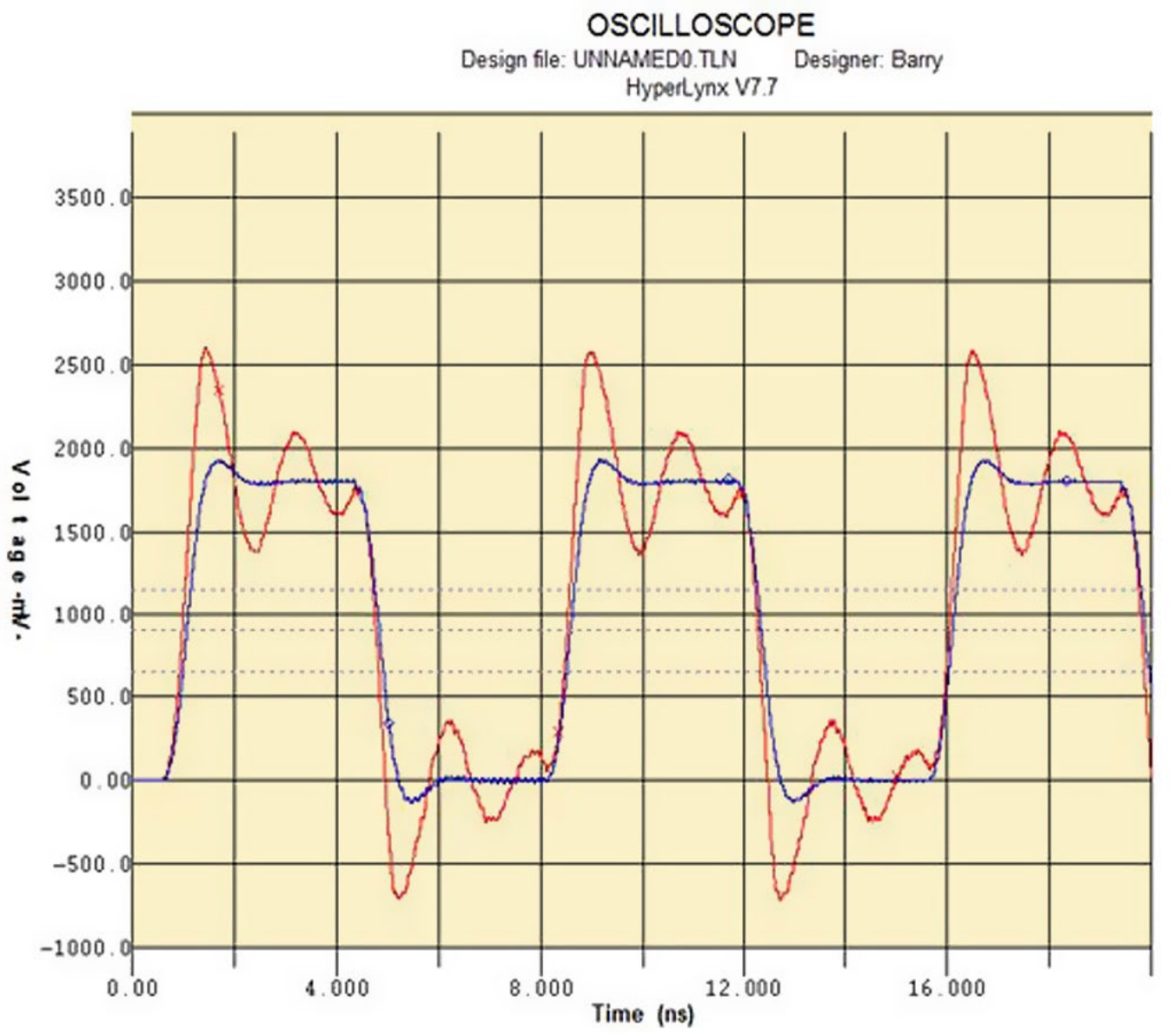

Figure 1: Unterminated (red) vs. terminated (blue) transmission lines.

For a microstrip transmission line with 3 mil dielectric thickness to ground, a 9 mil trace width is required to match a DDR3 34 ohm driver. Have you ever tried routing matched length DDR3 with 9 mil traces? That ain't gonna work. If the driver's impedance is even lower, say, 22 ohms, then you would need to route 15 mil traces.

Figure 2 illustrates the plot of impedance vs microstrip trace width (left) and impedance vs dielectric thickness (right). These plots are simulated by multiple passes of the field solver (in the background) to create heads-up graphs of how to adjust the particular variables to achieve the desired impedance. One can see that as the impedance goes down, the trace width increases to a point where it will be unroutable. Also, if we select too low of an impedance, the di/dt will increase, drawing excessive current from the supply and no doubt creating further power integrity issues.

So, it is a trade-off between trace width, trace (copper) thickness, dielectric thickness

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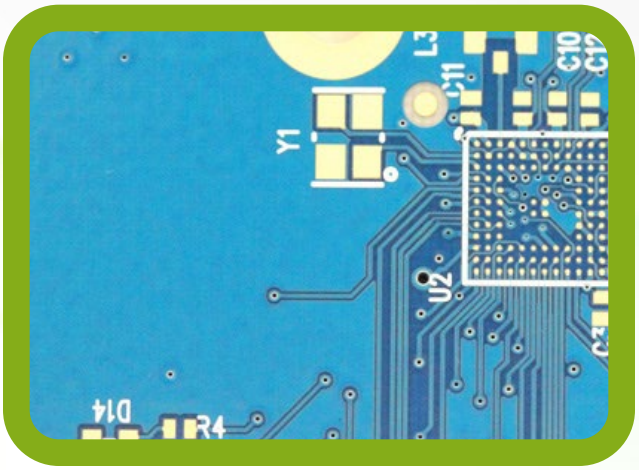

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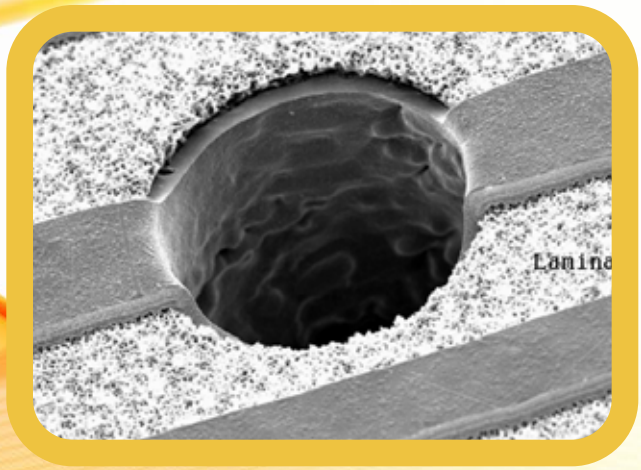

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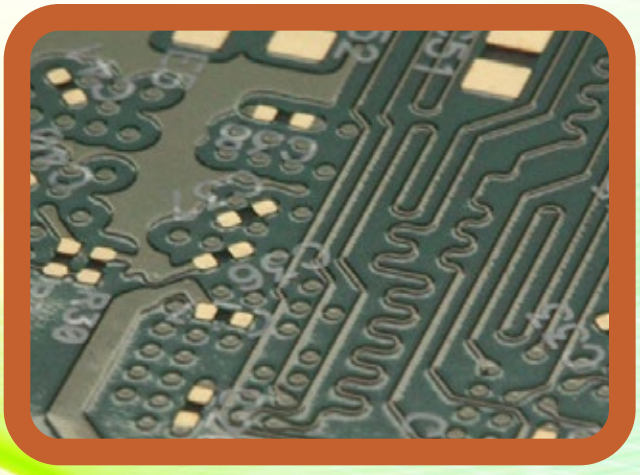

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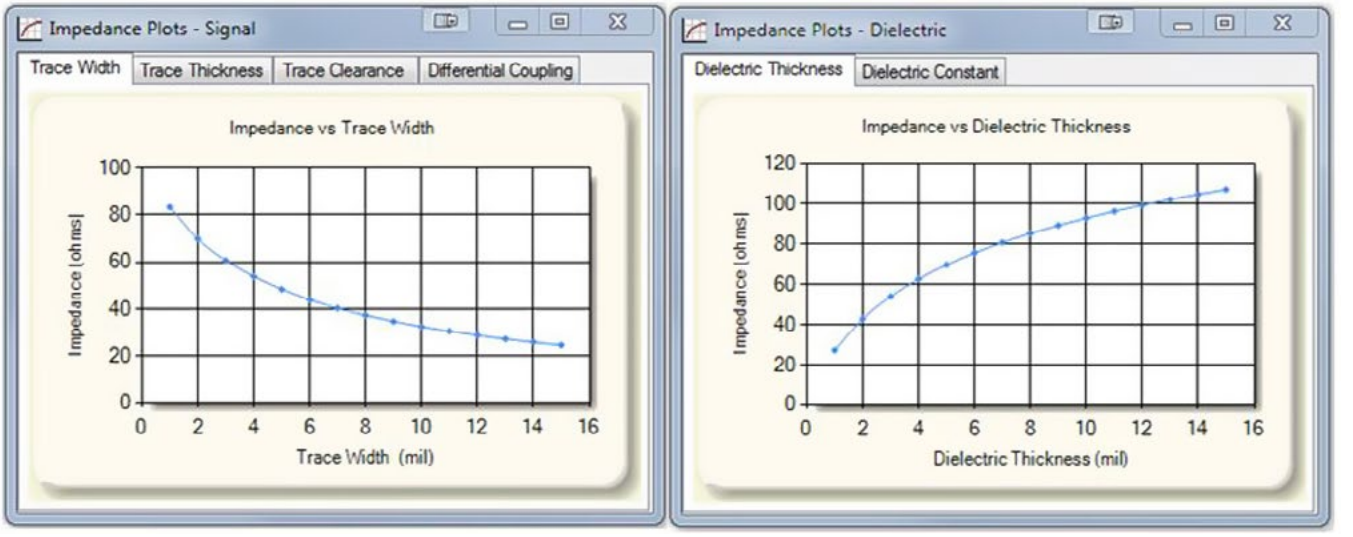


Figure 2: The ICD Stackup Planner's impedance plots.

and dielectric constant. Then if you also need to include differential impedance, the trace clearance also comes into play. Plus, one needs to also consider what the preferred fab shop has in stock. So determining the correct variable for your application is not as simple as clicking an impedance "goal-seeking" button. But rather, one should weigh up all the pros and cons of changing each variable and make an informed decision. That is exactly what the impedance plots allow you to determine.

Also, as the dielectric constant and loss of all materials varies with frequency, the impedance needs to be simulated at the frequency of the highest bandwidth taking into account the 5th harmonic. Traditional, dielectric constant and loss has been measured at 100MHz but these days a 1GHz (or higher) frequency is more appropriate to be used to determine the impedance.

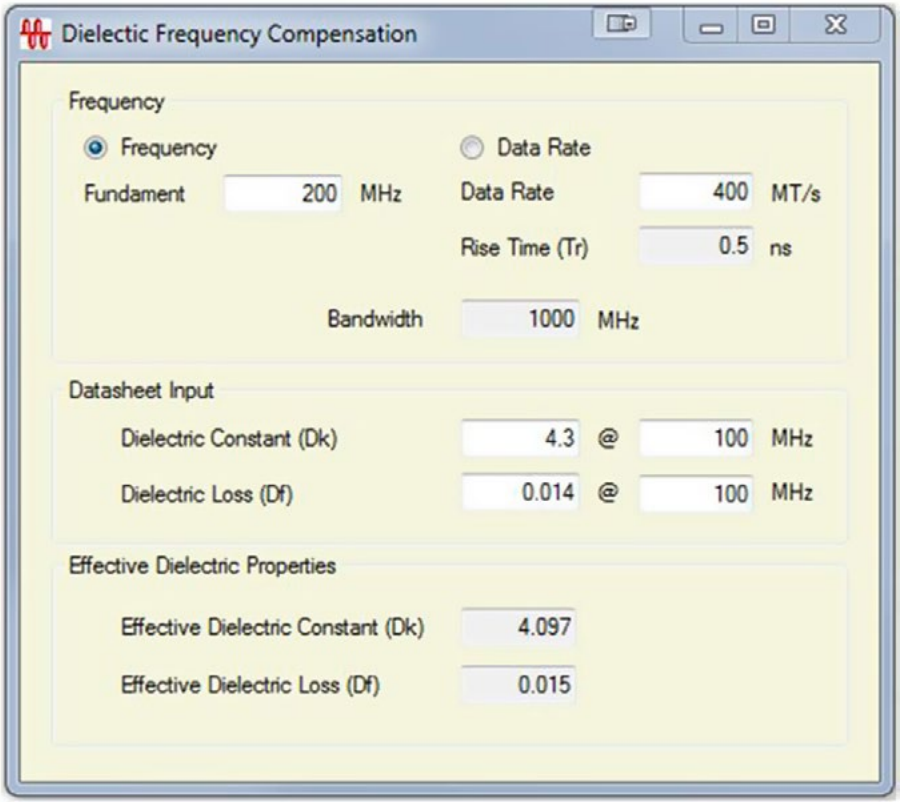
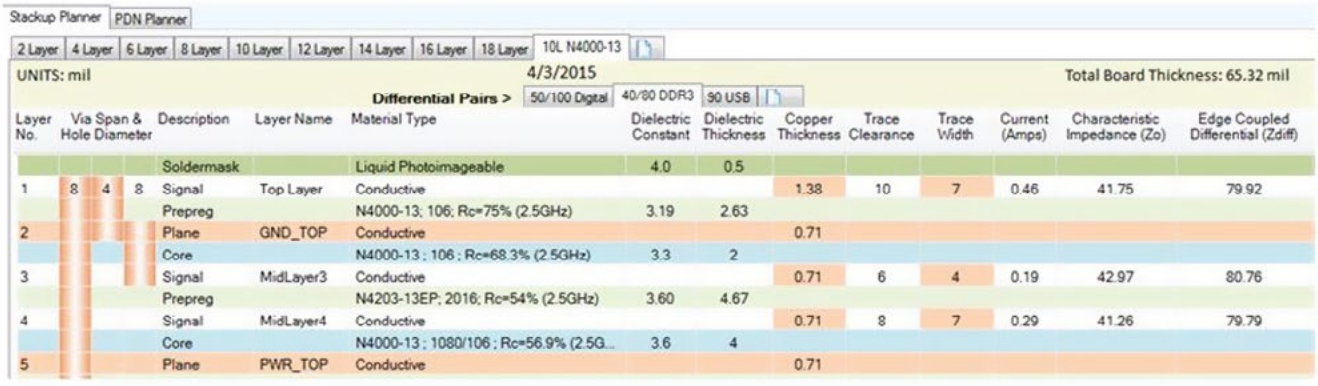


Figure 3: Calculation of effective dielectric constant and dielectric loss.

In Figure 3, a data rate of, say, 400MT/s or a fundamental frequency of 200MHz can be used to determine the maximum bandwidth. From



Stackup Planner | PDN Planner

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer | 10L N4000-13

UNITS: mil — 4/3/2015 — Total Board Thickness: 65.32 mil

Differential Pairs > 50/100 Digital | 40/80 DDR3 | 90 USB

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Liquid Photoimageable	4.0	0.5						
1	8 4 8	Signal	Top Layer	Conductive			1.38	10	7	0.46	41.75	79.92
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63						
2		Plane	GND_TOP	Conductive			0.71					
		Core		N4000-13 ; 106 ; Rc=68.3% (2.5GHz)	3.3	2						
3		Signal	MidLayer3	Conductive			0.71	6	4	0.19	42.97	80.76
		Prepreg		N4203-13EP; 2016; Rc=54% (2.5GHz)	3.60	4.67						
4		Signal	MidLayer4	Conductive			0.71	8	7	0.29	41.26	79.79
		Core		N4000-13 ; 1080/106 ; Rc=56.9% (2.5G...	3.6	4						
5		Plane	PWR_TOP	Conductive			0.71					

Figure 4: Multiple differential pair technologies per substrate.

that, the "effective" dielectric constant and loss can be extrapolated. Unfortunately, most material datasheets specify the dielectric constant (Dk) and dielectric loss (Df) at 100MHz. This is the traditional test parameter, however, that is now changing with the next generation of high-speed, low-loss laminates that are specified up to 10GHz or more. Some low loss microwave materials are measured at 100GHz.

Typically for a digital design, a characteristic impedance of 50–60 ohms is used. But, this becomes more important as the edge rates become faster and different technologies have their specific requirements. For example: Ethernet is 100 ohm and USB 90 ohms differential, DDR2 is 50/100 and DDR3/4 is 40/80 single-ended/differential impedance. So controlling impedance with a number of different technologies can become a challenge. Also, as operating voltages are reduced, the associated noise margins are also reduced, making it even more important to match the impedance.

Figure 4 illustrates the ICD Stackup Planner's unique differential pair calculation. In this case, digital, DDR3 and USB technologies are all accommodated on Nelco N4000-13, 2.5GHz material.

With differential impedance, there comes a (coupling) point whereby increasing the trace separation or the dielectric thickness has little or no further effect on impedance. At this point, the impedance rolls off and the traces become uncoupled. This is also the point where crosstalk of unrelated signals begins to occur. For the microstrip stackup of Figure 4, Figure 5 shows this differential coupling point at 8 mils. So, where I have a 10 mil trace clearance for the 79.92 ohms differential impedance, I should have backed this off to just 8 mil trace clearance in order to maintain sufficient coupling otherwise the two traces begin to act as individual single ended signals of 41.75 ohms.

For crosstalk, 8 mils (in this case) is also the minimum separation before coupling occurs. This gives you a defined clearance rule to constrain routing, in order to avoid edge coupled crosstalk of long parallel trace segments.

In conclusion, controlled impedance design is not just a matter of pushing a button to get the right trace width for the desired impedance. It is an interactive process of manipulating five variables in combination with the material your preferred fab shop stocks to achieve an educated result. Your product will not only be manufacturable, but also exhibit improved signal quality, reduced crosstalk and electromagnetic radiation and also perform reliably over many years.

Points to Remember

- A good transmission line is one that has constant impedance along the entire length of the line.
- The impedance of the driver must match the transmission line to avoid reflections.
- Drivers do not have the exact impedance to match the line (typically 10–35 ohms).
- Impedance matching slows down the rise and fall times, reduces the ringing (over/under-

CONTROLLED IMPEDANCE DESIGN *continues*

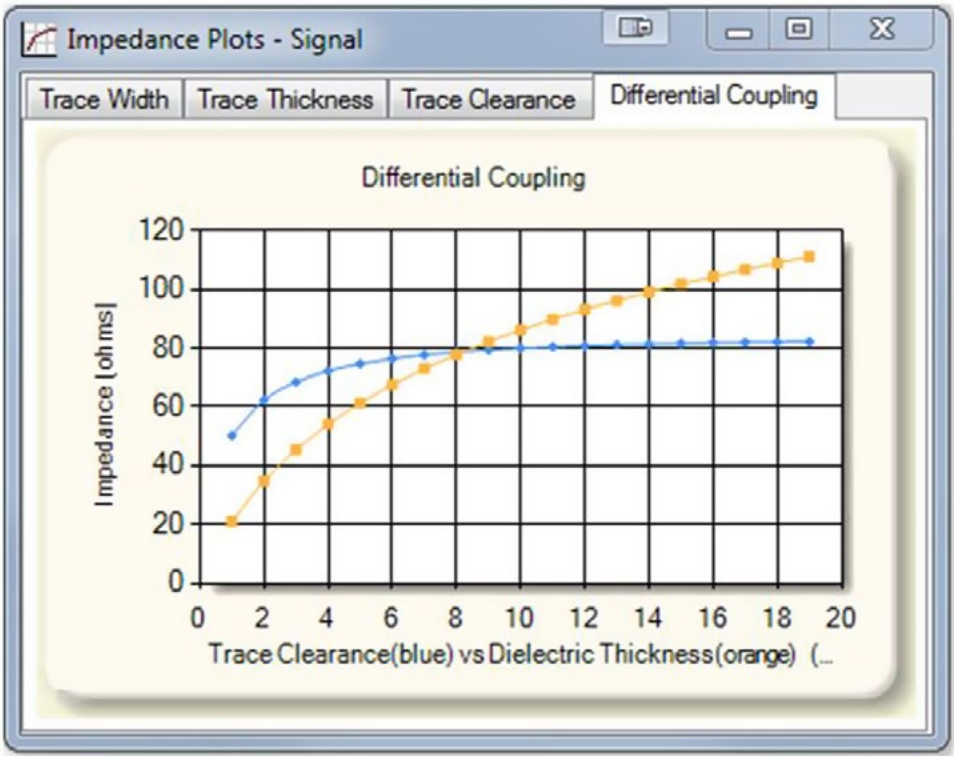


Figure 5: Multiple field solver passes produce differential coupling plot.

shoot) of clock drivers and enhances the signal quality of a high-speed design.

• Impedance plots are simulated by multiple passes of the field solver to create heads-up plots of how to adjust the particular variables to get the desired impedance.

• If you select too low of an impedance, the di/dt will increase, drawing excessive current form the supply and no doubt, creating further power integrity issues.

• Controlling impedance is a trade-off between trace width, trace (copper) thickness, dielectric thickness, dielectric constant and trace clearance.

• The dielectric constant and loss of all materials varies with frequency.

• Multiple differential pair technologies should be accommadated on the same substrate.

• The coupling point is where increasing the trace separation or the dielectric thickness has little or no further effect on differential impedance. At this point, the impedance rolls off and the traces become uncoupled. This is also the point where crosstalk of unrelated signals begins to occur. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Embedded Signal Routing, Impedance Matching.

3. Eric Bogatin, Signal and Power integrity Simplified.

4. Lee W. Ritchey, How and why of obtaining accurate impedance calculations.

5. The ICD Stackup and PDN Planner is available at: www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.

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The Do's and Don'ts of Signal Routing for Controlled Impedance

by Mark Thompson, C.I.D.
PROTOTRON CIRCUITS

In this column, we will once again be focusing on controlled impedance structures, both from the layout side and the simulation side. I will break them down into the sub-categories of the models they represent and the important points to remember when using the various models. I will also be asking questions such as, "Why would a fabricator ask for a larger impedance tolerance?" and "Where does the fabricator draw the line for controlling various structures?"

Later, I will break down my Top 10 do's and don'ts of signal routing.

A Few Rules of Thumb

Let's start with single-ended structures, both co-planar and those in "free space," i.e., not coupled to any adjacent copper pour.

For external single-ended structures starting with quarter or half-ounce copper, the trace width is typically about twice the dielectric needed between the impedance signal and its reference plane.

Example: A 4.25 mil trace needs about a .0026"–.0028" dielectric to be a reference plane for 50 ohms on half-ounce starting copper (1.5 ounces after plating).

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THE DO'S AND DON'TS OF SIGNAL ROUTING FOR CONTROLLED IMPEDANCE *continues*

Keep the copper pour that resides on the impedance layer a minimum of 3x the chosen trace width for impedance; this ensures no unwanted co-planar coupling occurs. At larger trace widths upwards of .012" this distance can be as little as 2x the trace width.

Differential Pairs

Be sure you match the lengths of each half of the differential pair. Make sure the same space is maintained throughout the run, with the exception of neck-down areas at the terminations.

Be careful when terminating differential pairs that you do not create same net space violations where smaller traces (neck-downs) terminate. See Figure 1.

Q: Why is this a problem?

A: If the same net space violation is LESS than the fabricator's specified minimum space value and the fabricator is not aware these neck-down areas are part of larger/longer differential pairs, they may "fill" the space violation.

Q. And why, exactly, is that a problem?

A. If a fabricator "fills" in the same net space violation, we have just changed the LENGTH of the differential pair!

Having said that, a fabricator will not solve for these small neck-down sections, only the larger, longer run of the same diff pair. This is true of SE structures as well. Really, anything less than about .3mm in length cannot be controlled to any great degree.

The same is true for surface single-ended or differential pairs that have the vast majority of the run on one layer and only pick up the diff pair on the opposing side in very short lengths.

What are some reasons a fabricator may ask for a wider impedance tolerance?

• For lines less than .1 mm: Here, many times a fabricator asks for +/-15%, but not because they think they are not going to hit the number. Remember that 10% of a .1 mm trace is 4/10 of a mil, less than half a mil! Hence many shops ask for 15% for traces .004" and below.

• Additionally, the fabricator may ask for 15% due to less-than-predictable surface finishes. Let's say the part has either epoxy-filled or silver-epoxy-filled vias and the fabricator is outsourcing. The epoxy or silver-fill process itself requires that the material be pushed into the holes under pressure. After curing, they typically "planarize," basically grinding down the surface so it is flat, and herein lies the rub. If the planarization process is not perfect, there can be quarter to half a mil difference end-to-end on the surface topography, making it more difficult to properly predict impedances.

The 10 Do's and Don'ts

1. **Do** consult with your fabricator regarding any controlled impedances at your earliest pos-

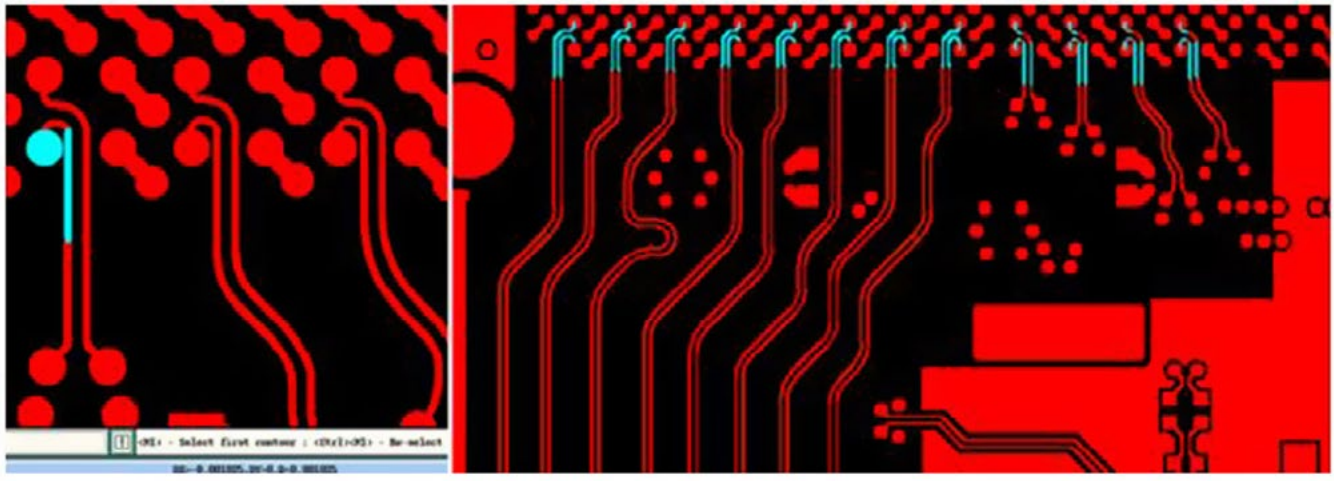

Figure 1: Differential pairs create same net spacing violation at termination points.

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THE DO'S AND DON'TS OF SIGNAL ROUTING FOR CONTROLLED IMPEDANCE *continues*

sible convenience. **Don't** assume that specifying "dielectric only" will meet your impedance requirements.

2. **Do** make sure your diff pairs have the same space throughout the run and are of matched length. **Don't** assume the odd-mode impedance is half the differential pair value.

3. **Do** keep copper 3x the trace width away from the impedance trace if no co-planar coupling is wanted. **Don't** vary the ground separation distance on the same layer. Keep all the ground separation distances the same on a given layer for all co-planar impedances.

4. **Do** ensure that all structures have a proper reference plane. **Don't** place differential pairs over large splits on a plane layer.

5. **Do** remember Dk decreases as frequency increases. **Don't** assume that all shops know this.

6. **Do** stick to calling out the desired material by its 4101/ number. **Don't** assume all materials are the same.

7. **Do** add any bumps in differential pairs, in an effort to match lengths, somewhere away from the terminations. **Don't** wrap around a termination point, creating same net spacing violations.

8. **Do** terminate traces in the center of the pad. **Don't** terminate traces at the edge of the pad or device.

9. **Do** consult your fabricator for minimum routing gaps for the desired copper weight. **Don't** rely on data sheets alone for proper Dk and Df info at a specific speed.

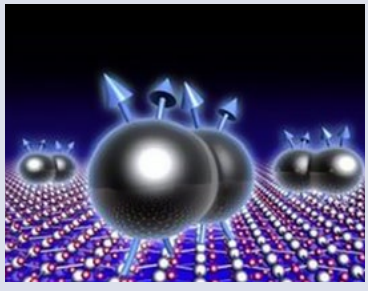
10. **Do** make sure that what you have specified on the drawing for impedance trace widths actually exists. **Don't** call out impedances solely by their net names.

Please feel free to contact me with any questions or comments. **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. His column, *The Bare (Board) Truth,* appears bimonthly in *The PCB Design Magazine.* To read past columns, or to contact Thompson, click here, or phone 425-823-7000, ext. 239.

New Stream for Topological Quantum Computer Research

Heterointerfaces composed of dissimilar materials have been applied to transistors and LEDs. In particular, the best-quality electron system is formed in gallium arsenide heterostructures, where a unique quantum phase was found at low temperature about 30 years ago. This quantum phase is expected to be applied for a new type of topological quantum computer which possesses dramatically improved computing speed while maintaining tolerance for computational error.



Researchers at the Quantum Phase Electronics Center/Department of Applied Physics, the Graduate School of Engineering at the University of Tokyo, headed by Professor Masashi Kawasaki, in collaboration with a group headed by Dr. Jurgen Smet at the Max Planck Institute, have fabricated ZnO heterostructures of unprecedented high quality, and observed the quantum phase in a material other than a GaAs heterostructure for the first time.

This research has been published in the online edition of Nature Physics.

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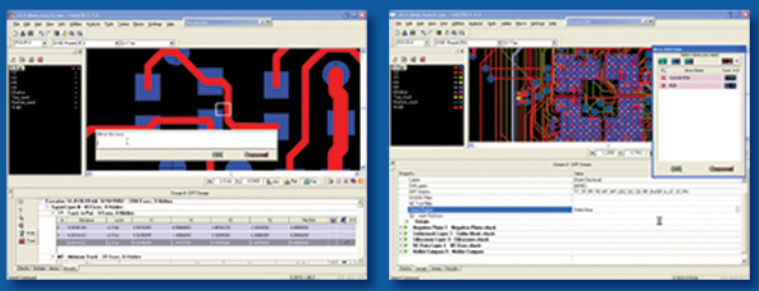

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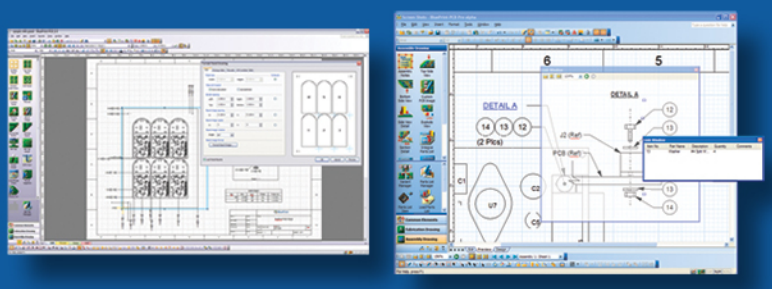

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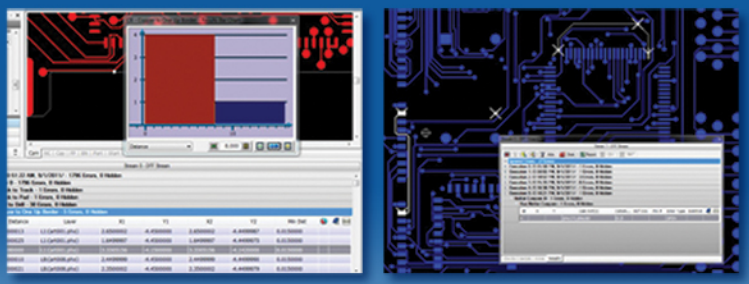

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Impedance Control, Revisited

by Martyn Gaudion
POLAR INSTRUMENTS

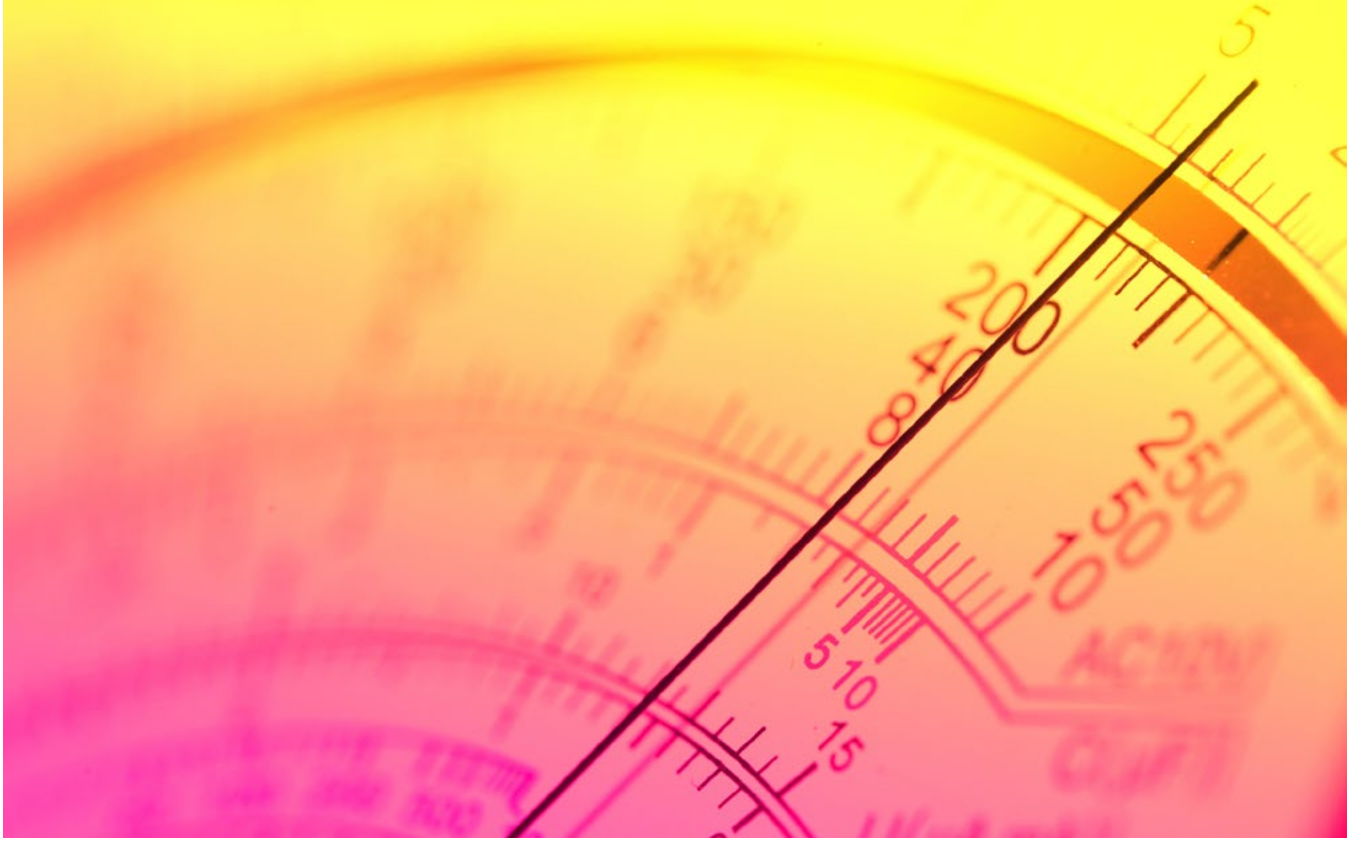
Surprising me on a regular basis is the way that demand for impedance control continues to extend into a broader range of product. After some 20 years of involvement in this field, I would have expected that everyone who needed to consider impedance control would have the capability nailed. Fortunately, that's not the case, and a steady stream of "how to" questions keep coming my way.

The positives for new fabricators and designers lie in the fact that, even though impedance control may be new to them, there is a wealth of information available. Some of this information is common sense and some is a little counterintuitive. So, this month I'd like to go back to the fundamentals, and even if you are an experienced hand at the subject, it can be worth revisiting the basics from time to time.

Standards

It's worth remembering that traceable reference impedance standards are available and all impedance measurement systems should be able to be compared to a traceable standard. The reference air line is the de facto standard for impedance—a precision manufactured coaxial standard "air" referring to the fact that air is employed as the dielectric in this type of precision reference line.

Because a closed-form equation exists for the impedance of a coaxial structure, air lines may be calibrated by national standards bodies who can strip down the line and make precise measurements of the internal diameter of the outer body and the external diameter of the inner conductor. The bore measurement is usually made with a technique called air gauging,



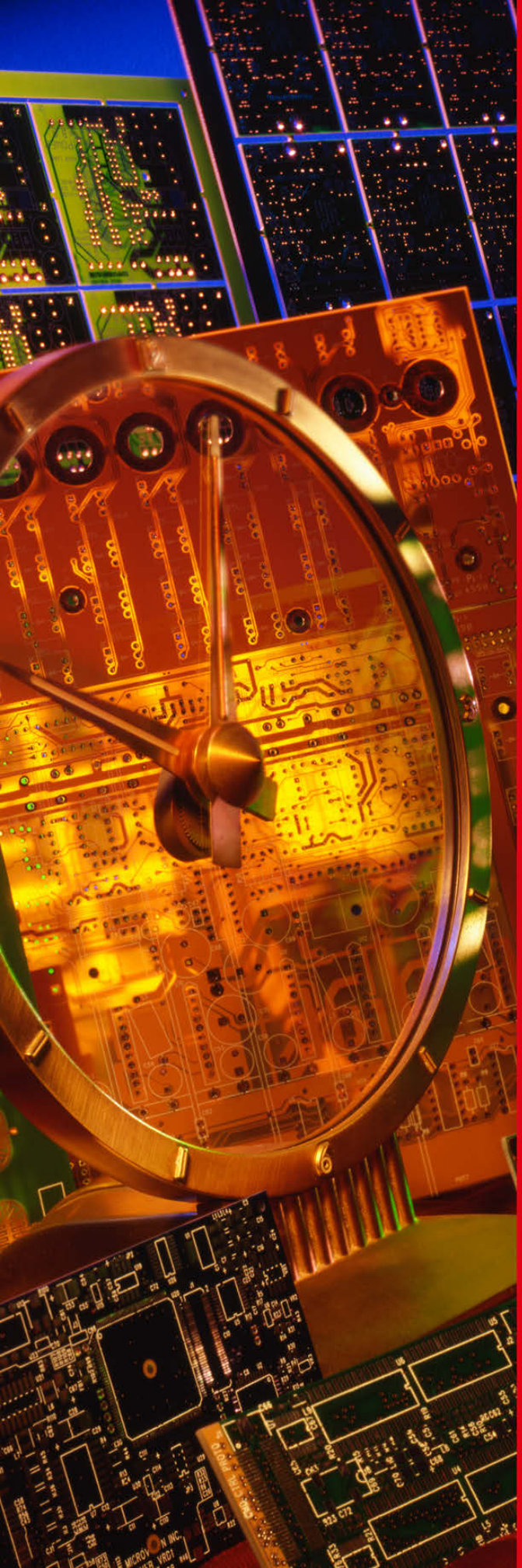


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Figure 1: Traceable 50 ohm air line standard with SMA adaptor.

which involves inserting a precision piston into the bore and measuring the resistance to air passing through the piston into the bore. It's a science in its own right and an interesting subject if you happen to be into mechanical metrology.

Now, back on track with impedance. The availability of air line standards allows measurement systems manufacturers to prove accuracy traced back to a national standard. Air lines are commonly available in impedances of 50, 75, and 100 ohms, and, more rarely, 28 ohm air lines.

Why 28 ohms? Well, this was the impedance of Rambus RAM data lines, and back in the day when that technology was introduced the impedance requirements were demanding and led to 28 ohm air lines being developed as a standard for that application. A side benefit of the availability of 28 ohm lines is the ability to traceably calibrate a TDR over a very broad range of commonly used impedances. At a lower cost, but also providing an economic alternative to air lines, semi-rigid precision coax can be used as a transfer standard and has the benefit of robustness if used in a production environment.

Expectations

Newcomers to impedance control are sometimes tempted to tie down specifications more tightly than is practical. Perhaps this arises because the units of lossless impedance are ohms, and it is customary to expect that something specified in ohms (resistance) can be specified very tightly indeed. However, you have to remember that impedance is in fact a high-frequency characteristic of a transmission line, and in general the higher the frequency gets the less realistic it is to think you can specify down to fractions of an ohm or less. In fact, the traceable air line standards mentioned earlier in this article may have an uncertainty of 0.2–0.5 ohms, and that's for a reference line possibly costing many hundreds of dollars. So you would not expect a line based on the finest geometry possible on an FR-4 board to come even close to those levels. Often impedance is ±10%; tighter specs may demand ±5% and some critical applications may be more tolerant of higher or lower impedances—so you may encounter specs of say 50 ohms +7 ohms – 4 ohms, for example.

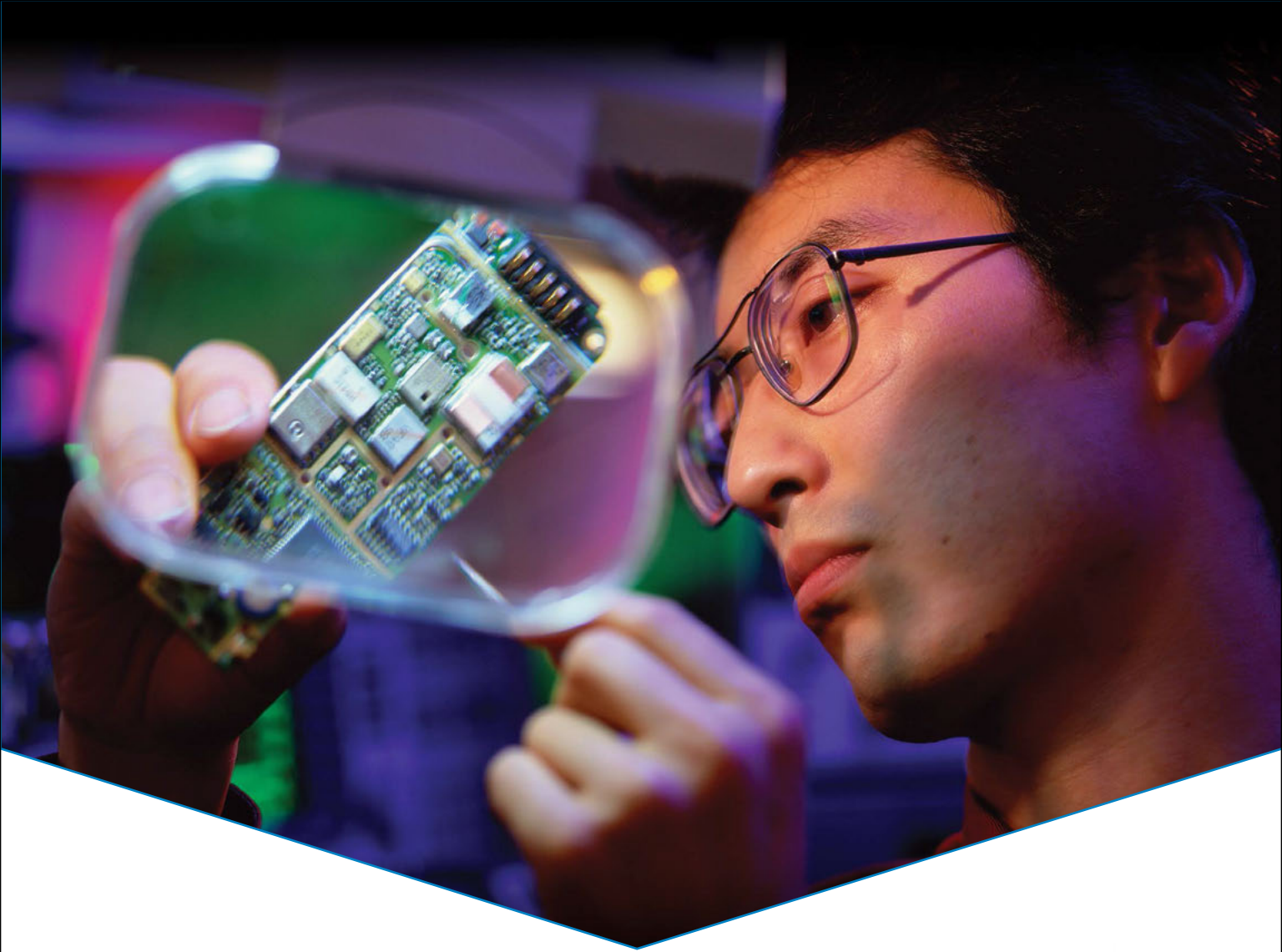
Test coupons

As frequency increases the test coupon (sometimes called the test vehicle) becomes an increasingly important part of the measurement system as, coincidentally, do the probes and the interconnect cables to the measurement system. Careful design of the coupon ensures that artefacts which could spoil the measurement quality are minimised.

Launch pad diameter is a compromise between ease of probing and launch aberrations; having a coupon that is long enough (IPC still specifies 6"/150 mm) gives an adequate sample of the trace to measure over a reasonable length of PCB; after all, the impedance test is meant to measure the consistency as well as the absolute value of the fabricated impedance. Also, coupons should be designed to ensure that any nomenclature in the copper is well away from the trace under test and that the transmission lines are back away from the coupon edges to avoid any effects on impedance from the proximity of the edge of the ground plane. Likewise, on the coupon power and ground planes should be interconnected—but not on the PCB itself!

Modelling

Coaxial standards can be calculated with precise closed loop equations. However, PCB transmission lines are far from uniform cylindrical coaxial structures. At their simplest they could be regarded as rectangular traces over infinite planes, and whilst approximations do exist for calculating the basic variations of such structures, they are limited when pushed to modern trace geometries, which leaves you requiring a field solver if you wish to make ac-



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IMPEDANCE CONTROL, REVISITED *continues*

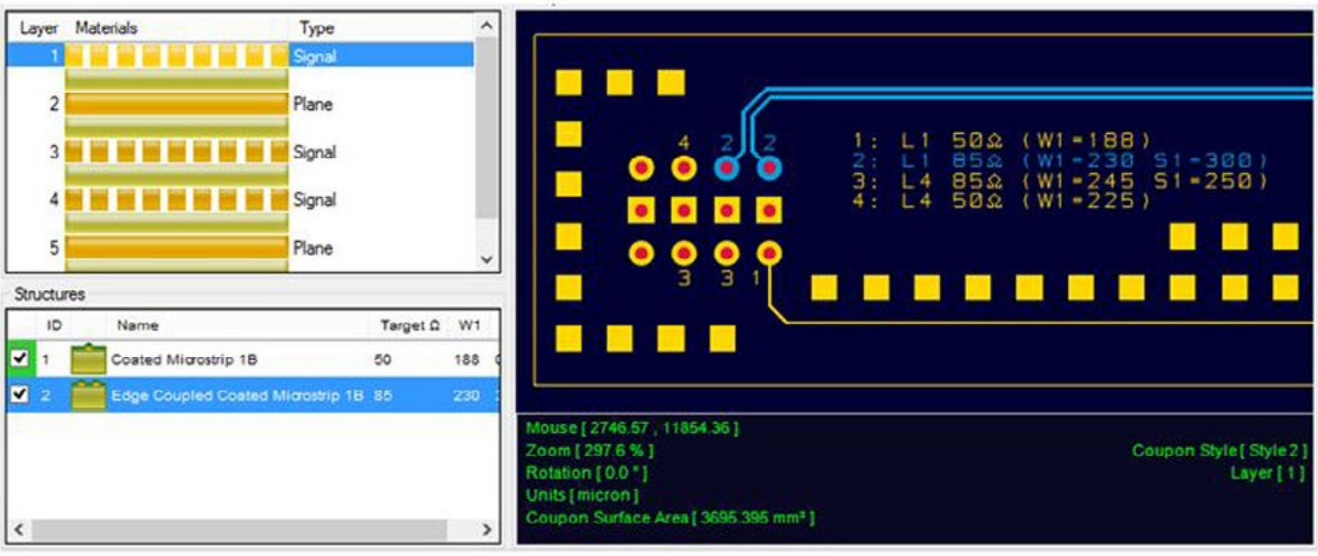


Figure 2: Impedance coupon generation software.

curate calculations. All solvers obey the laws of physics and for the same data in should give the same impedance out. When choosing a solver you should look for one that permits you to model the layered substructure of the PCB, take into account the trapezoidal nature of the traces and where possible account for resin rich layers or areas of resin richness between differential pairs. The ability to run sensitivity analysis is a useful enhancement too.

Modelled vs. Measured

The aim of modelling is to get you as close to the desired result in the shortest number of iterations, ideally, right first time; it is worth keeping an open mind when looking at correlation of measured vs modelled impedance. Modelling predicts the uniform impedance of a uniform trace in a homogenous medium. It's good to ask yourself a few questions when faced with less correlation than you expect. First, never assume anything. Look at both the measured and modelled and see if there are areas which need attention; often, a 5 or 10 ohm mismatch between modelled and measured can be comprised of an ohm here an and ohm there. And you can suddenly find 5 or 6 ohms hiding from your initial assumptions.

First, did you assume you made what you think you made? A microsection is a wise step to confirm actual geometries. Second, look at the impedance trace—does it slope? This could be from trace taper or, on thin traces, trace resistance. Or does it dip at the start or the end, implying that the coupon design or the setting of test limits is not optimised? On the modelling side, has the trapezoidal shape of the trace been considered? Have you run sensitivity analysis to see which trace parameter has the largest contribution to any error? Attention to the above makes you better prepared to optimise correlation on the next spin. I mentioned sloping traces: if not down to taper, this could be because you are using sub 75 micron lines on thin copper—and here you would need to consider measuring instantaneous impedance using a technique such as launch point extrapolation.

Occasionally Expect the Unexpected

From time to time you might experience results that seem too consistent. This was the experience of one of our fabricator customers who accidentally set a TDR to measure the end of the cable and not the coupon. Unsurprisingly, the TDR reported very repeatable results all within a fraction of 50 ohms. If your measurements are too consistent, you might be measuring the wrong thing; for example, another fabricator customer etched the PCB part number in the ground plane

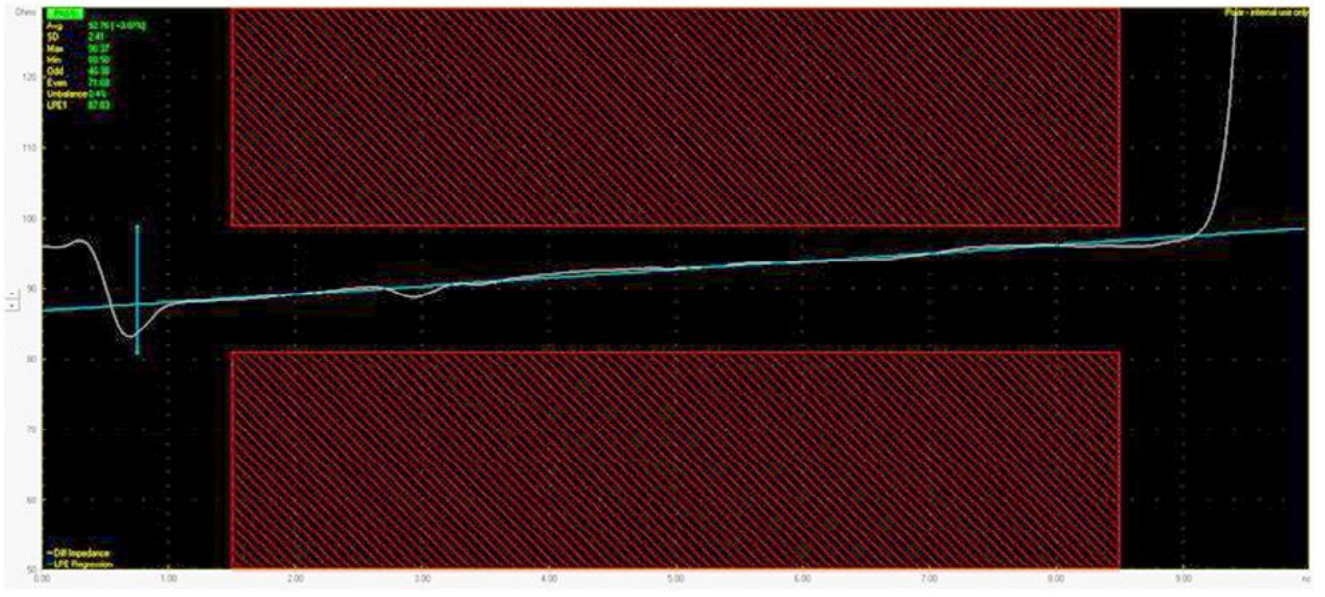


Figure 3: Incident impedance measurement by LPE method. (For more detail, see my February 2015 column, I3: Incident, Instantaneous, Impedance).

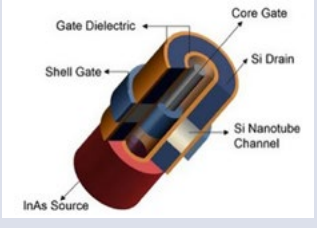
over a stripline structure, causing the impedance to increase because of the lack of copper in the return path. As with any measurement system, awareness of what to expect and what not to expect and having the tools to predict what ought to be happening are essential to providing reliable and consistent results. **PCBDESIGN**

Martyn Gaudion is CEO of Polar Instruments. To contact him, click here.

Novel Nanotube Tunnel FET Architecture

Classical semiconductor physics suggests that a single charge transport CMOS (complementary metal-oxide–semiconductor) device cannot achieve ultra-high-performance and ultra-low-standby-power at the same time. Nanoelectronics researchers are trying to design devices that hit the 'sweet spot', i.e. where a charge transport device can provide its highest performance at its lowest power consumption, especially in its 'off' state.

Now, researchers from the Integrated Nanotechnology Lab at King Abdullah University of Science and Technology (KAUST) show a unique device concept which combines the advantages of a tunnel field-effect transistor (TFET) for ultra-low OFF (leakage) current and ultra-steep sub-threshold slope for sharper and faster ON and OFF switching due to the FET's nanotube architecture.



In addition, this nanotube device, which is built on heterogeneous material systems, shows scalability and area efficiency in an unprecedented way. According to the scientists, this is the highest comprehensive functionality achieved ever in single device.

"We capitalized on an innovative design of nanotube architecture with a core (inner) gate and a shell (outer) gate," Muhammad Mustafa Hussain, an Associate Professor of Electrical Engineering at KAUST, tells Nanowerk. "This way we were able to achieve utmost electrostatic control for ultra-low-standby-power operation."

The team reports their findings in the April 29, 2015 online edition of Scientific Reports ("InAs/Si Hetero-Junction Nanotube Tunnel Transistors").

PCB007 Highlights

Multek CTO Excited about the Challenges of Fast-Moving Wearables Market

I-Connect007 Publisher Barry Matties and recently-appointed Multek CTO Dr. Joan Vrtis sat down at IPC APEX EXPO to discuss the rapidly evolving wearables market, especially for medical, and the myriad questions that must be addressed. Other topics include Multek's contribution to the wearables industry and what it sees as the main challenges to putting their circuits into various applications.

Raising a Unified Voice for an Advanced Manufacturing Economy

The electronics manufacturing industry is an important sector in the global economy, and John Hasselmann, VP of Government Relations at IPC, is an advocate for policies that will help our industry as well as the prosperity and welfare of billions of people.

Reliability and Harmonization of Global Standards at Forefront of EIPC Efforts

At IPC APEX EXPO 2015, I-Connect007 Technical Editor Pete Starkey caught up with EIPC's Michael Weinhold and Alun Morgan, who were happy to discuss both recent and ongoing focuses for EIPC. Also touched on was the importance of the alignment of global standardization processes, especially for Asia.

Are There Advantages to Changing Your Registration System?

I-Connect007 Publisher Barry Matties recently had a conversation with DIS's Tony Faraci at IPC APEX EXPO 2015, to learn more about their pinless registration system. What was most interesting to Matties was the potential advantages a pinless system offers and why the process has not been widely adopted.

Schmoll Keeping an Eye on the Future—and on LDI

In this interview, Thomas Kunz, who has been at the helm of Schmoll Maschinen as president since 1993, discusses the company's lengthy history in mechanical engineering (more than 70 years), current global scope, and what he sees as a steady progression in directions that make the most sense to customers, which includes laser direct imaging.

Bernie Kessler: Pioneering Spirit Then and Now

I-Connect007's Patty Goldman sat down with long time friend and IPC Hall of Famer Bernie Kessler at IPC APEX EXPO 2015 in San Diego. Among other things, the two discussed the early days of IPC and the origins of APEX EXPO.

Manz: A Total Process Solution

At the recent CPCA Show in China, I-Connect007 Publisher Barry Matties had a chance to speak with Alex Liu, the deputy general manager of the PCB business unit for Manz. Manz has focused on creating a process from direct imaging to wet processing. With more entrants into the direct imaging arena, Liu feels that this approach gives Manz and their customers an advantage.

ESI's New Gemstone Changing the Rules for Laser

I-Connect007 Publisher Barry Matties sat down at CPCA 2015 with ESI's Mike Jennings, who explained the company's newest addition: Gemstone, an ESI-designed and manufactured laser system with 10,000 guaranteed hours, which is poised to change the rules in flex and other printed circuit processing.

Key PCB Makers Strategize to Meet Industry Demands

The computer/peripheral application is expected to witness the highest growth followed by the communication applications. Nippon Mektron, Zhen Ding Technology Holding Limited, Young Poong Electronics Co. Ltd., Unimicron Technology Corp., and Samsung Electro-Mechanics are among the major suppliers of PCBs.

N.A. PCB Book-to-Bill Ratio Strengthens

"Although North American PCB sales continued slightly below last year's levels in February, bookings strengthened," said Sharon Starr, IPC's director of market research. "This increased the book-to-bill ratio…it has been in positive territory for the past five months, which is a positive indicator for sales growth in the first half of 2015."

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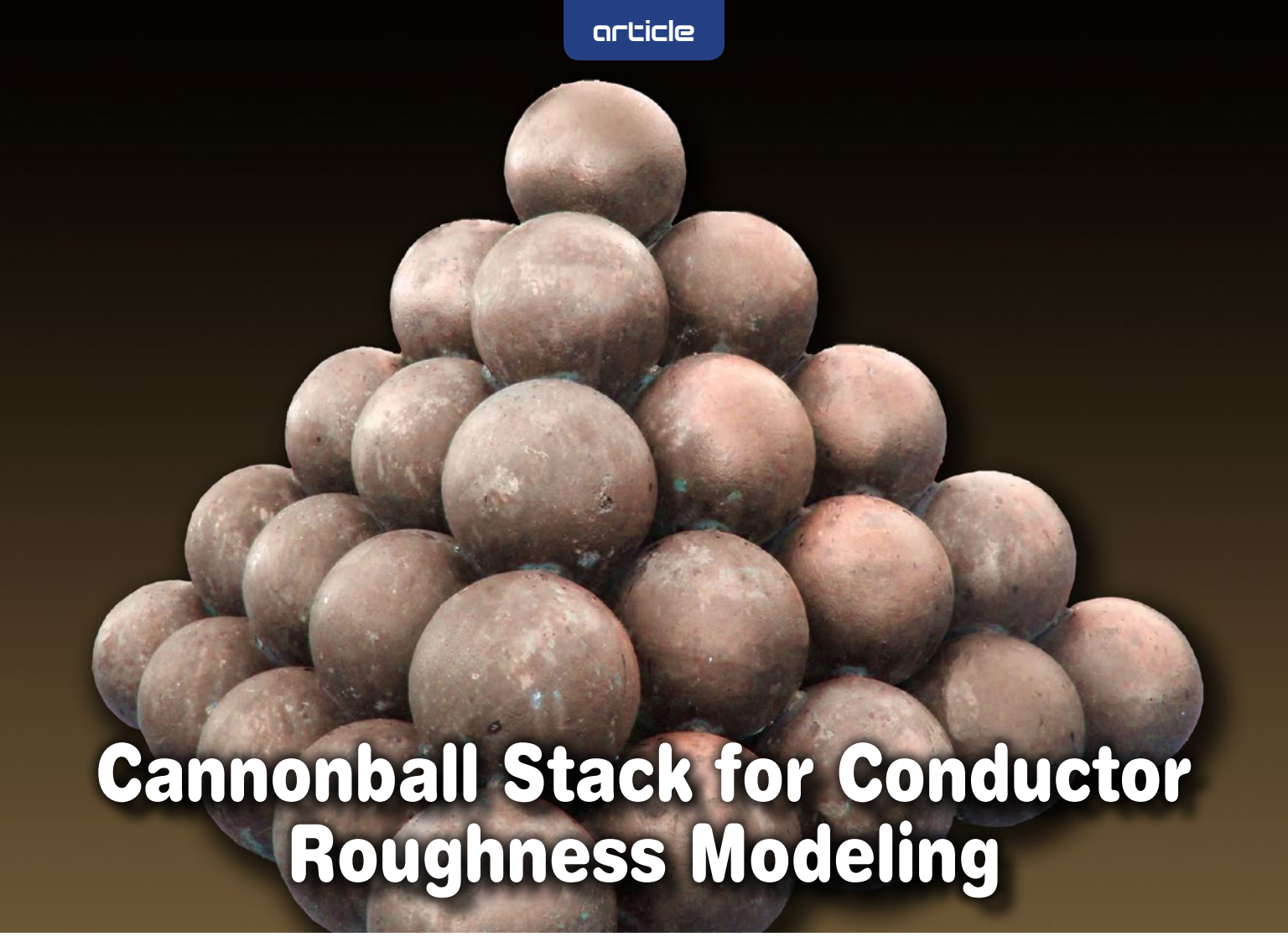

Cannonball Stack for Conductor Roughness Modeling

by Bert Simonovich
LAMSIM ENTERPRISES

In the GB/s regime, accurate modeling of conductor losses is a precursor to successful high-speed serial link designs. Failure to model roughness effects can ruin you day. For example, Figure 1 shows the simulated total loss of a 40-inch PCB trace without roughness compared to measured data. Total loss is the sum of dielectric and conductor losses. As can be seen, with just -3dB delta in insertion loss between simulated and measured data at 12.5 GHz, there is half the eye height opening with rough copper at 25GB/s.

According to Wikipedia, close-packing of equal spheres is defined as "a dense arrangement of congruent spheres in an infinite, regular arrangement (or lattice)" [8]. The cubic close-packed and hexagonal close-packed are examples of two regular lattices. The cannonball stack is an example of a cubic close-packing of equal spheres, and is the basis of modeling the surface roughness of a conductor in this article.

So what do cannonballs have to do with modeling copper roughness anyway? Well, other than sharing the principle of close packing of equal spheres, and having a cool name, not very much.

Background

In PCB construction, there is no such thing as a perfectly smooth conductor surface. There is always some degree of roughness that promotes adhesion to the dielectric material. Unfortunately this roughness also contributes to additional conductor loss.

Electro-deposited (ED) copper is widely used in the PCB industry. The manufacturing process sees a large rotating drum, made of polished stainless steel or titanium, which is partially submerged in a bath of copper sulfate solution. The cathode terminal is attached to the drum,

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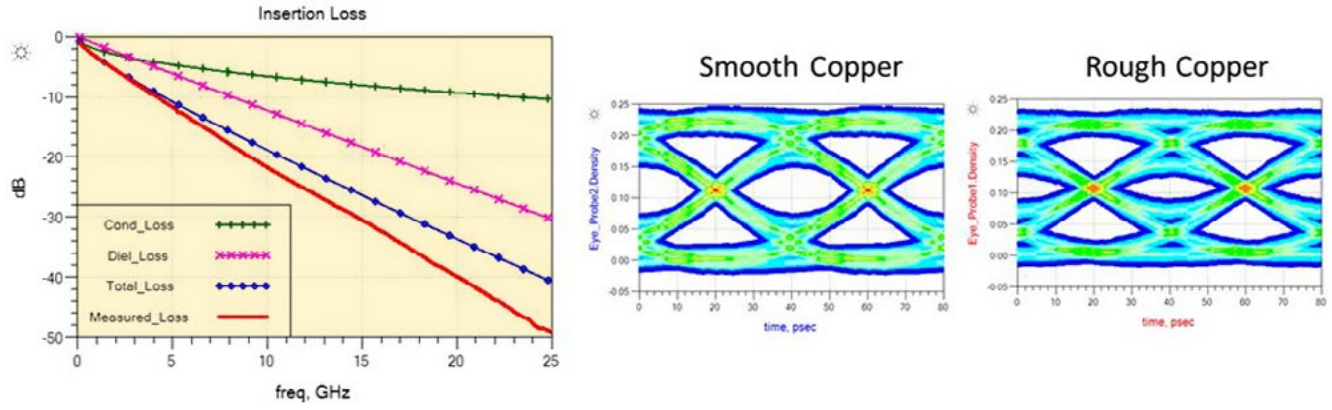

Figure 1: Comparisons of measured insertion loss of a 40-inch trace vs simulation. Eye diagrams show that with -3dB delta in insertion loss at 12.5 GHz there is half the eye opening at 25GB/s. Modeled and simulated with Keysight EEsof EDA ADS software.

while the anode terminal is submerged in the solution. A DC voltage supplies the anode and cathode with the correct polarity.

As the drum slowly rotates, copper is deposited onto it. A finished sheet of ED copper foil has two sides. The matte side faces the copper sulfate bath, while the drum side faces the rotating drum. Consequently, the drum side is always smoother than the matte side.

The matte side is usually attached to the prepreg sheets, prior to final pressing and curing, to form the core laminate. Prepreg is the term commonly used for a weave of glass fiber yarns pre-impregnated with resin which is only partially cured. To enhance adhesion, the matte side has additional treatment applied to roughen the surface. For high frequency boards, sometimes the drum side of the foil is laminated to the core. In this case it is referred to as reversed treated (RT) foil. Even after treatment, it is still smoother than standard treated foils.

Various foil manufacturers offer ED copper foils with varying degrees of roughness. Each supplier tends to market their product with their own brand name. Presently, there seems to be three distinct classes of copper foil:

- Standard
- Very-low profile (VLP)
- Ultra-low profile (ULP) or profile free (PF)

Some other common names referring to ULP class are HVLP or eVLP.

In lieu of scanning electron microscopy (SEM) analysis, profilometers are often used to quantify the roughness tooth profile of electrodeposited copper. Tooth profiles are typically reported in terms of 10-point mean roughness (R_z) for both sides, but sometimes the drum side reports average roughness (R_a) in manufacturers' data sheets. Some manufacturers also report RMS roughness (R_q).

Modeling Roughness

Several modeling methods were developed over the years to determine a roughness correction factor (K_{sr}). When multiplicatively applied to the smooth conductor attenuation (α_{smooth}), the attenuation due to roughness (α_{rough}) can be determined by:

$$\alpha_{rough} = K_{SR}\alpha_{smooth} \qquad \text{Equation 1}$$

The most popular method, for years, has been the Hammerstad and Jensen (H&J) model, based on work done in 1949 by S. P. Morgan. The H&J model assumes a triangular corrugated surface, representing the tooth structure of rough copper. It was thought that when the skin depth is small, compared to the tooth height, current begins to flow along the corrugated surface; thereby increasing its loss due to the longer path length. However, the theory breaks down from a physics perspective because there is no evidence of additional time delay

(TD), compared to the fixed spatial length of the trace.

The H&J roughness correction factor (K_{HJ}), at a particular frequency, is solely based on a mathematical fit to S. P. Morgan's power loss data and is determined by [2]:

$$K_{HJ} = 1 + \frac{2}{\pi}\arctan\left(1.4\left(\frac{\Delta}{\delta}\right)^2\right)$$ Equation 2

Where:
K_{HJ} = H&J roughness correction factor;
Δ = RMS tooth height in meters;
δ = skin depth in meters.

Alternating current (AC) causes conductor loss to increase in proportion to the square root of frequency. This is due to the redistribution of current towards the outer edges caused by skin-effect. The resulting skin-depth (δ) is the effective thickness where the current flows around the perimeter and is a function of frequency.

Skin-depth at a particular frequency is determined by:

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}}$$ Equation 3

Where:
δ = skin-depth in meters;
f = sine-wave frequency in Hz;
μ_0= permeability of free space =1.256E-6 Wb/A-m;
σ = conductivity in S/m. For annealed copper σ = 5.80E7 S/m.

The model has correlated well for microstrip geometries up to about 15 GHz, for surface roughness of less than 2 RMS. However, it proved less accurate for frequencies above about 5 GHz for very rough copper [3].

In recent years, the Huray model [4] has gained popularity due to the continually increasing data rate's need for better modeling accuracy. It takes a real-world physics approach to explain losses due to surface roughness. The model is based on a non-uniform distribution of spherical shapes resembling snowballs and stacked together forming a pyramidal geometry, as shown by the SEM photo in Figure 2.

Figure 2: SEM photograph of electrodeposited copper nodules on a matte surface resembling snowballs on top of heat treated base foil. Photo credit Oak-Mitsui.

By applying electromagnetic wave analysis, the superposition of the sphere losses can be used to calculate the total loss of the structure. Since the losses are proportional to the surface area of the roughness profile, an accurate estimation of a roughness correction factor (K_{SRH}) can be analytically solved by [1]:

$$K_{SRH}(f) = \frac{A_{matte}}{A_{flat}} + \frac{3}{2}\sum_{i=1}^{j} \frac{\left(\frac{N_i \times 4\pi a_i^2}{A_{flat}}\right)}{\left(1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2}\right)}$$ Equation 4

Where:
K_{SRH} (f) = roughness correction factor, as a function of frequency, due to surface roughness based on the Huray model;
$\frac{A_{matte}}{A_{flat}}$ = relative area of the matte base compared to a flat surface;
a_i = radius of the copper sphere (snowball) of the i^{th} size, in meters;
$\frac{N_i}{A_{flat}}$ = number of copper spheres of the i^{th} size per unit flat area in sq. meters;
δ (f) = skin-depth, as a function of frequency, in meters.

The design feedback method [7], as illustrated in Figure 3, is another practical way to model conductor roughness and extract material properties. The idea here is to design and fabricate a test coupon using the dielectric material and copper foil roughness you plan on using in the final design. After measuring and cross-sectioning a sample, you would bring this data into a circuit simulator, and then fit the simulation to match insertion loss and phase. You would then use the extracted parameters in your real design simulation and finally designing the actual product.

Although this method is quite practical and accurate, obtaining good measured data requires considerable effort. First a high level of expertise is required to design the test coupon. Next expensive test equipment and skill is required in the measurement and de-embedding of the fixture. Finally, considerable expertise and know-how is needed to tune the right parameters such that the final model fits both insertion loss and phase. All this adds up to increased time and dollars, and is beyond the scope and resources of many companies.

Cannonball Model

This leads us to the Cannonball model. Using the concept of cubic close-packing of equal spheres, the radius of the spheres (ai) and tile area (A_{flat}) parameters for the Huray model can now be determined solely by the roughness parameters published in manufacturers' data sheets.

This model is a follow-up research to my recent DesignCon2015 paper titled Practical Method for Modeling Conductor Surface Roughness Using Close Packing of Equal Spheres [1]. In that paper I presented a similar model using hexagonal close-packing of equal spheres.

Since losses are proportional to the surface area of the roughness profile, the Cannonball model can be used to optimally represent the surface roughness. As illustrated in Figure 4, there are three rows of spheres stacked on a

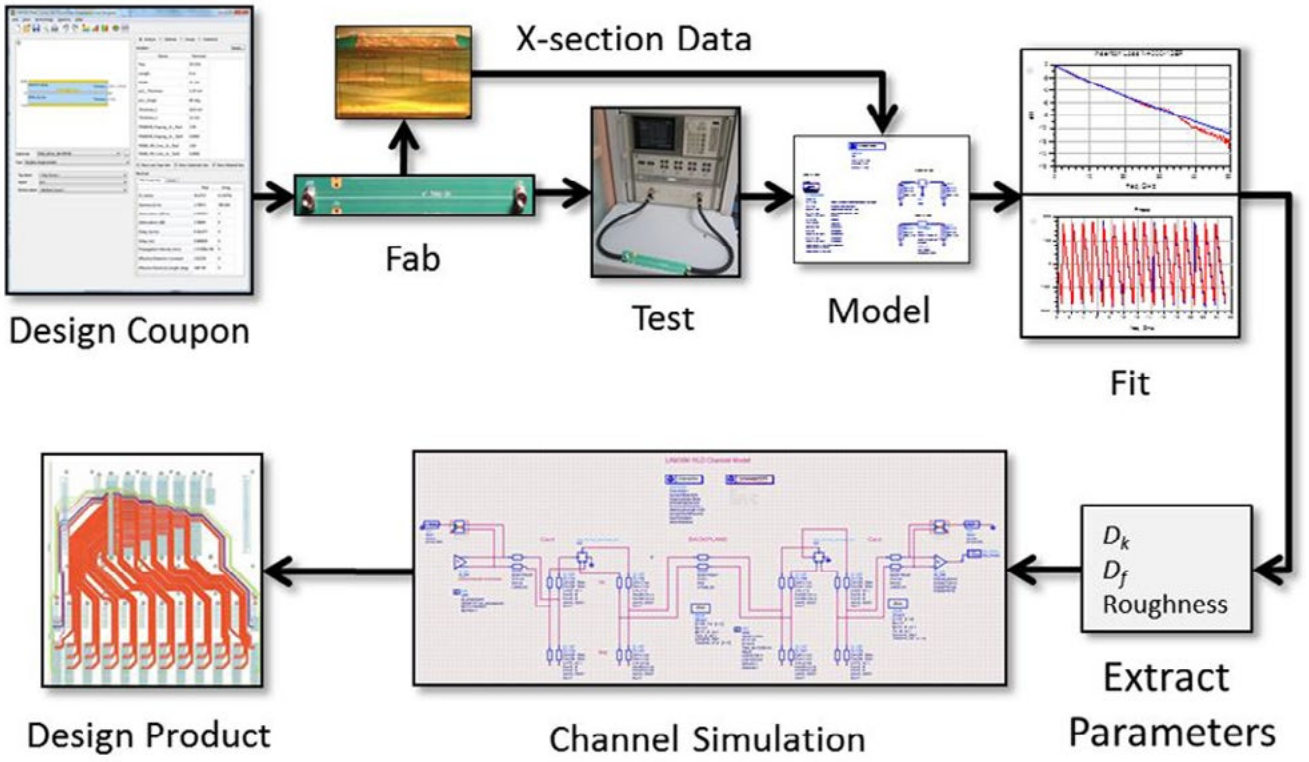

Figure 3: Design feedback method to determine material parameters.

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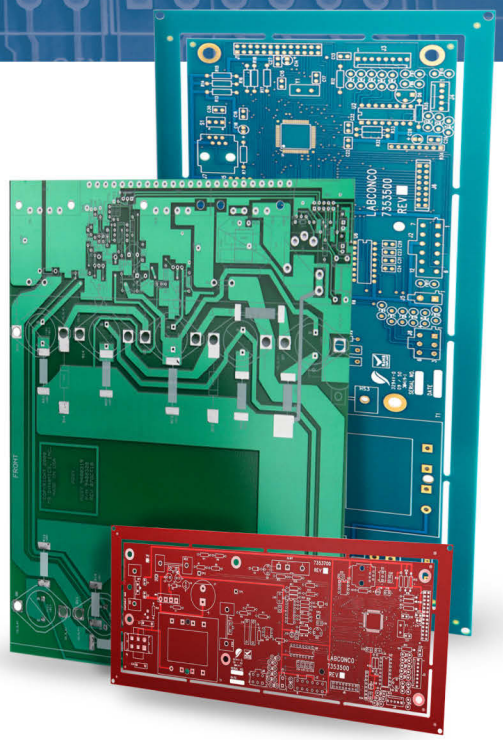

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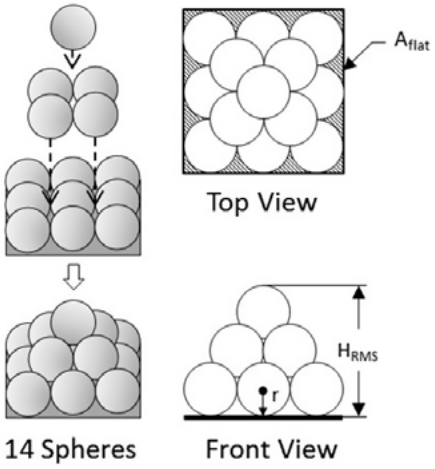

Figure 4: Cannonball model showing a stack of 14 uniform size spheres (left). Top and front views (right) shows the area (A_{flat}) of base, height (H_{RMS}) and radius of sphere (r).

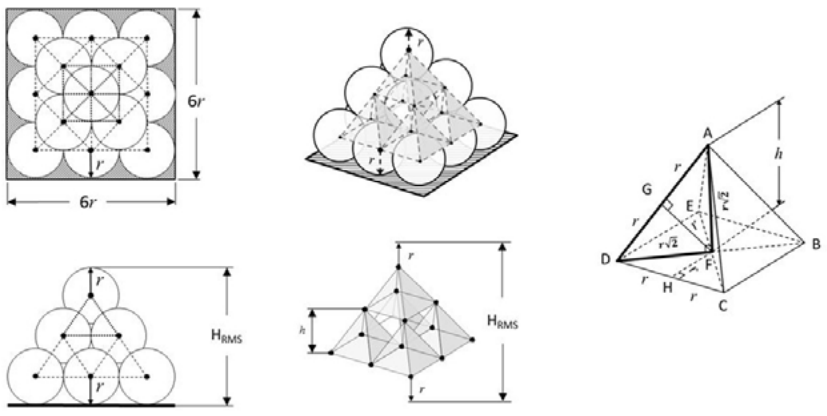

Figure 5: Cannonball model with pyramid lattice structure. Five pyramids form a stacked lattice structure connecting the centers of all 14 spheres. Total height (H_{RMS}) equals the stacked height of 2 pyramids plus the diameter (2r) of a single sphere.

square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top.

Because the Cannonball model assumes the ratio of A_{matte}/A_{flat} = 1, and there are 14 spheres, Equation 4 can be simplified to:

$$K_{SR}(f) = 1 + 84\left(\frac{\left(\frac{(\pi r^2)}{A_{flat}}\right)}{\left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2r^2}\right)}\right)$$

Equation 5

Where:

K_{SR} (f) = roughness correction factor, as a function of frequency, due to surface roughness based on the Cannonball model;

r = sphere radius in meters; δ (f) = skin-depth, as a function of frequency in meters;

A_{flat} = area of square tile base surrounding the 9 base spheres in sq. meters.

As shown in Figure 5, there are 5 square-based pyramids connecting the centers of all 14 spheres forming a stacked lattice structure. A single pyramid, labeled ABCDE, is shown for reference.

Given that each side of the pyramid ABCDE = 2r, it can be shown that:

$$h = r\sqrt{2}$$

Since:

$$H_{RMS} = 2r + 2h$$
$$= 2r\left(1 + \sqrt{2}\right)$$

Then the radius of a single sphere is:

$$r = \frac{H_{RMS}}{2\left(1 + \sqrt{2}\right)}$$

And the area of the square flat base is:

$$A_{flat} = (6r)^2$$

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You can approximate the RMS heights of the drum and matte sides by Equations 6 and 7:

$$H_{RMS\_drum} \approx \frac{R_{z\_drum}}{2\sqrt{3}} \quad \text{Equation 6}$$

Where: R_{z_drum} is the 10-point mean roughness in meters. If the data sheet reports average roughness, then R_{a_drum} is used instead.

$$H_{RMS\_matte} \approx \frac{R_{z\_matte}}{2\sqrt{3}} \quad \text{Equation 7}$$

Where: R_{z_matte} is the 10-point mean roughness in meters.

Practical Example

To test the accuracy of the model, board parameters from Yuriy's Shlepnev's February 2014 article in *The PCB Design Magazine* [5] was used. Measured data was obtained from Simbeor software design examples courtesy of Simberian Inc. [9]. The extracted de-embedded generalized modal S-parameter (GMS) data was computed from 2-inch and 8-inch single-ended stripline traces. They were originally measured from the CMP-28 40 GHz High-Speed Channel Modeling Platform from Wild River Technology [15].

The CMP-28 Channel Modeling Platform, shown in Figure 6, is a powerful tool for development of high-speed systems up to 40 GHz, and is an excellent platform for model development and analysis. It contains a total of 27 microstrip and stripline interconnect structures. All are equipped with 2.92mm connectors to facilitate accurate measurements with a vector network analyzer (VNA).

The PCB was fabricated with Isola FR408HR material and reverse treated (RT) 1oz. foil. The dielectric constant (Dk) and dissipation factor (Df), at 10 GHz for FR408HR 3313 material, was obtained from Isola's isoStack web-based online design tool [10]. This tool is free, but you need to register to use it. An example is shown in Figure 7.

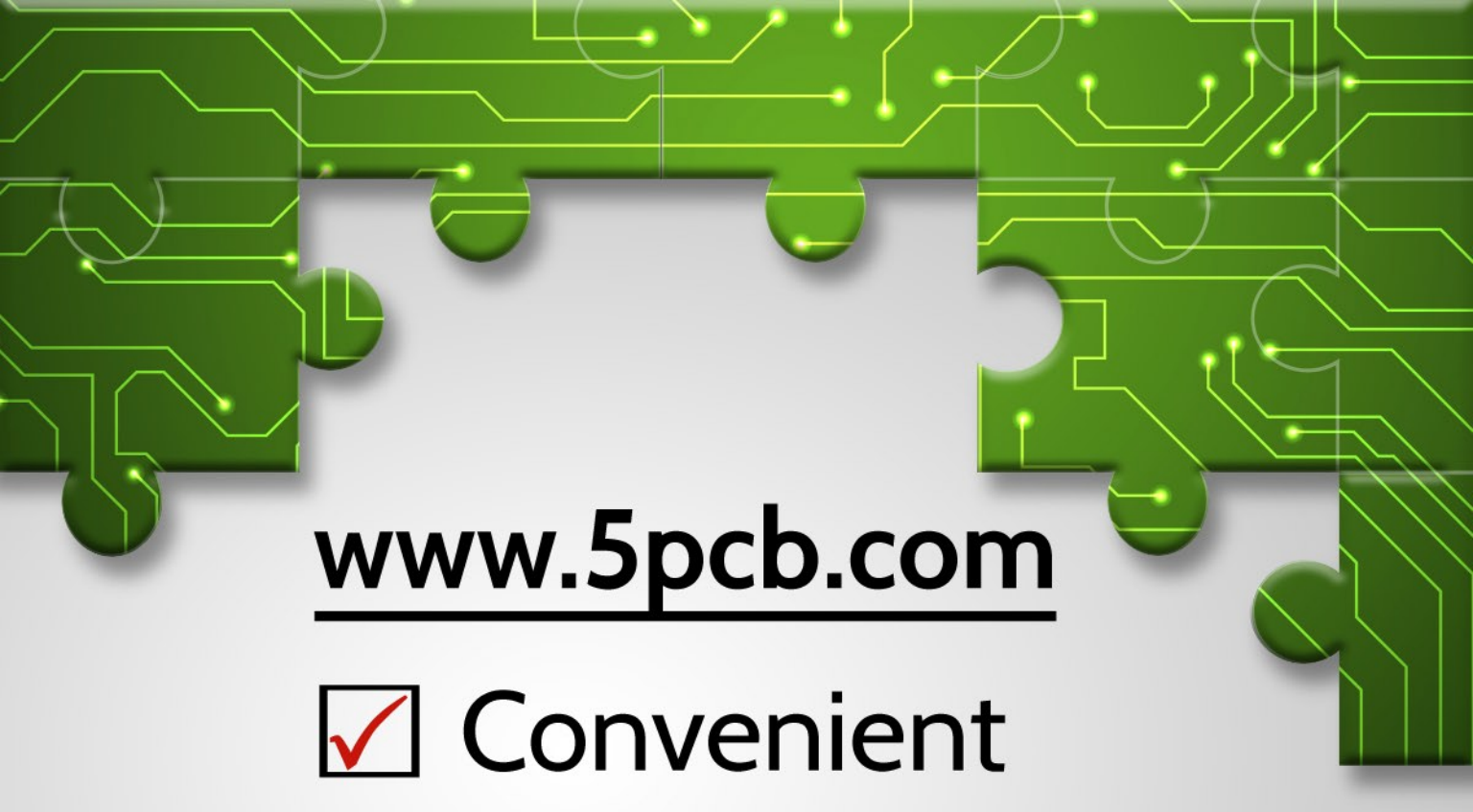
Figure 6: CMP-28 Modeling Platform from Wild River Technology. Photo credit Wild River Technology.

isoStack

Design name: CMP28	Total number of cores: -1	Number of signal layers: 1	Length unit: mils	Frequency 10GHz
Date: Sat Mar 28 2015 12:08:48	Total pressed thickness: 39.900	Number of reference planes: 3		

	Thickness		Ref. plane	Zo	Diff Z	Tpd	Width	Spacing	Fill	Weight	Dk	Df	Build	Type
1	1.400		true	na	na	na	5.000	10.000	100	1				
	10.600										3.59	0.0095	3x3313-57.0	FR408HR
2	1.250		false	49.0	98.0	161	10.380	10015.000	5	1				
	12.000										3.65	0.0094	3x3313	FR408HR
3	1.250		true	na	na	na	5.000	10.000	100	1				

Figure 7: Example of Isola's isoStack online software used to determine dielectric thicknesses, *Dk, Df* and characteristic impedance for the CMP-28 board.



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Typical traces usually have a trapezoidal cross-section after etching due to etch factor. Since the tool does not handle trapezoidal cross-sections in the impedance calculation, an equivalent rectangular trace width was determined based on a 2:1 etch-factor (60 degree taper). The as designed nominal trace width of 11 mils, and a 1oz trace thickness of 1.25 mils per isoStack was used in the analysis.

The default foil used on FR408HR core laminates is MLS, Grade 3, controlled elongation RT foil. The roughness parameters were easily obtained from Oak-Mitsui [11]. Reviewing the data sheet, 1 oz. copper roughness parameters R_z for drum and matte sides are 120 µin (3.175 µm) and 225 µin (5.715 µm) respectively. Because this is RT foil, the drum side is the treated side and bonded to the core laminate.

An oxide or micro-etch treatment is usually applied to the copper surfaces prior to final lamination. This provides enhanced adhesion to the prepreg material. CO-BRA BOND® [12] or MultiBond MP [13] are two examples of oxide alternative micro-etch treatments commonly used in the industry. Typically 50 µin (1.27 µm) of copper is removed when the treatment is completed. But depending on the board shop's process control, this can be 70-100 µin (1.78-2.54 µm) or higher.

The etch treatment creates a surface full of micro-voids which follows the underlying rough profile and allows the resin to squish in and fill the voids providing a good anchor. Because some of the copper is removed during the micro-etch treatment, we need to reduce the published roughness parameter of the matte

Parameter	FR408HR
Dk Core/Prepreg	3.65/3.59 @10 GHz
Df Core/Prepreg	0.0094/0.0095 @ 10 GHz
R_z Drum side	3.175 µm
R_z Matte side before Micro-etch	5.715 µm
R_z Matte side after 50 µin (1.27 µm) Micro-etch	4.443 µm
Trace Thickness, *t*	31.730 µm
Trace Etch Factor	2:1 (60 deg taper)
Trace Width, w	11 mils (279.20 µm)
Core thickness, H1	12 mils (304.60 µm)
Prepreg thickness, H2	10.6 mils (269.00 µm)
GMS trace length	6 in (15.23 cm)

Table 1: CMP-28 test board parameters obtained from manufacturers' data sheets and design objective.

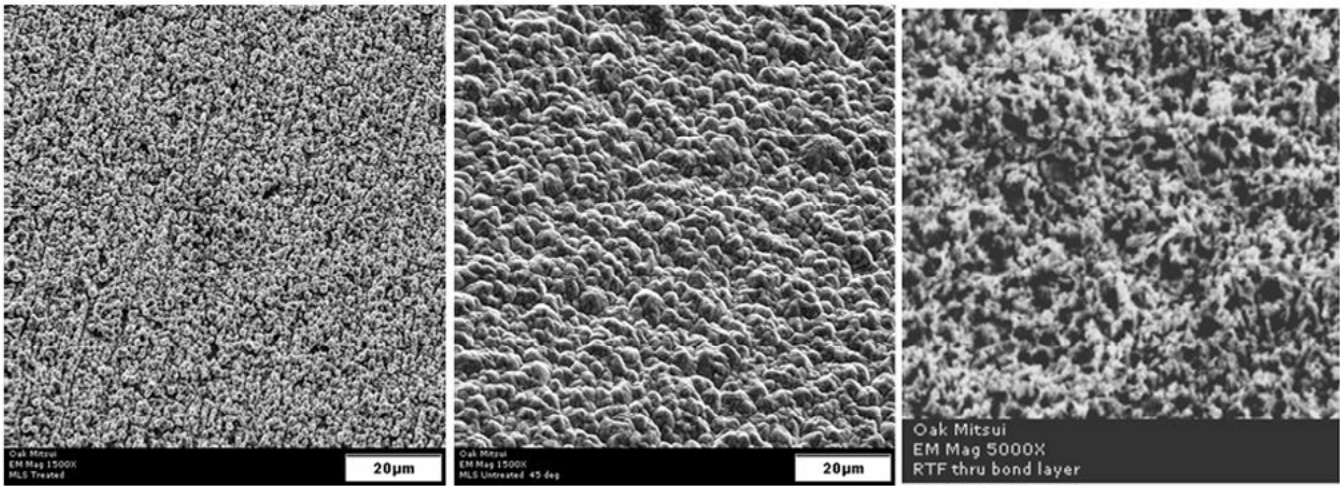


Figure 8: Example SEM photos of MLS RT foil. Left is the treated drum side and center is untreated matte side. SEM photo on the right is the matte side after etch treatment. (source Oak Mitsui)

side by nominal 50 µin (1.27 µm) for a new roughness of 175 µin (4.443 µm).

Figure 8 shows SEM photos of typical surfaces for MLS RT foil courtesy of Oak-mitsui. The left and center photos are the treated drum side and untreated matte side respectively. The right photo is a 5000x SEM photo of the matte side showing micro-voids after micro-etch treatment.

The data sheet and design parameters are summarized in Table 1. Respective Dk, Df, core, prepreg and trace thickness were obtained from the isoStack software, shown in Figure 7. Roughness parameters were obtained from the Oak-Mitsui data sheet. R_z of the matte side after micro-etch treatment (R_z = 4.443µm) was used to determine K_{sr_matte}.

Keysight EEsof EDA ADS software [14] was used for modeling and simulation analysis. A controlled impedance line (CIL) enhancement in version 2015.01 makes modeling the transmission line substrate easy. Unlike earlier substrate models, the CIL model allows you to model trapezoidal traces.

Figure 9 is the general schematic used for analysis. There are three transmission line substrates; one for dielectric loss; one for conductor loss and the other for total loss without roughness.

Dielectric loss was modeled using the Svensson/Djordjevic wideband Debye model to ensure causality. By setting the conductivity parameter to a value much-much greater than the normal conductivity of copper ensures the conductor is lossless for the simulation. Similarly the conductor loss model sets the Df to zero to ensure lossless dielectric.

Total insertion loss (IL) of the PCB trace, as a function of frequency, is the sum of dielectric and rough conductor insertion losses.

$$IL_{rough}(f) = K_{SR\_avg}(f)\left(IL_{smooth}(f)\right) + IL_{diel}(f)$$

Equation 8

To accurately model the effect of roughness, the respective roughness correction factor (K_{sr}) must be multiplicatively applied to the AC resistance of the drum and matte sides of the traces separately. Unfortunately ADS, and many other commercial simulators, do not allow access to these surfaces to apply the correction properly. The best you can do is to apply the average of (K_{SR_drum}) and (K_{SR_matte}) side to the smooth conductor loss (IL_{smooth}), as described above.

The following are the steps to determine K_{SR_avg} (f) and total IL with roughness:

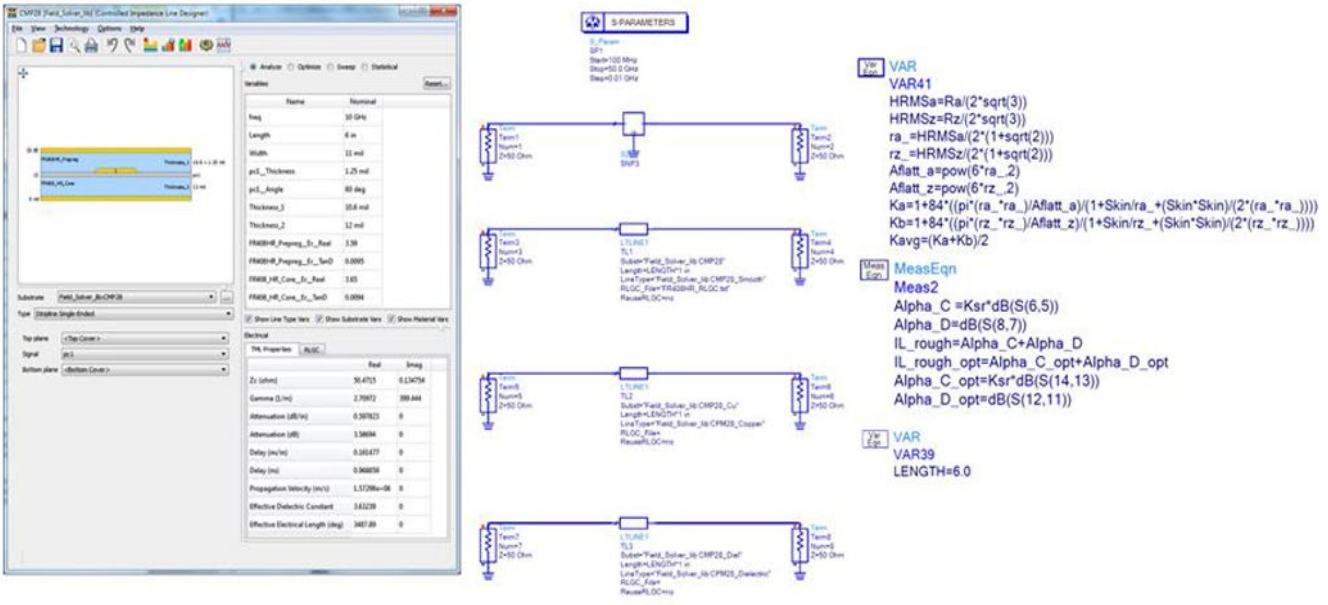


Figure 9: Keysight EEsof EDA ADS generic schematic of controlled impedance line designer used in the modeling and simulation analysis.

1. Determine H_{RMS_drum} and H_{RMS_matte} from Equation 6 and Equation 7.

$$H_{RMS\_drum} \approx \frac{R_{z\_drum}}{2\sqrt{3}};\quad H_{RMS\_matte} \approx \frac{R_{z\_matte}}{2\sqrt{3}}$$

2. Determine the radius of spheres for drum and matte sides:

$$r_{drum} = \frac{H_{RMS\_drum}}{2\left(1+\sqrt{2}\right)};\quad r_{matte} = \frac{H_{RMS\_matte}}{2\left(1+\sqrt{2}\right)}$$

3. Determine the area of the square flat base for drum and matte sides:

$$A_{flat\_drum} = \left(6r_{drum}\right)^2;\quad A_{flat\_matte} = \left(6r_{matte}\right)^2$$

4. Determine $K_{SR\_drum}(f)$ and $K_{SR\_matte}(f)$:

$$K_{SR\_drum}(f) = 1 + 84\left(\frac{\left(\frac{\left(\pi r_{drum}^2\right)}{A_{flat\_drum}}\right)}{\left(1+\frac{\delta(f)}{r_{drum}}+\frac{\delta^2(f)}{2r_{drum}^2}\right)}\right)$$

$$K_{SR\_matte}(f) = 1 + 84\left(\frac{\left(\frac{\left(\pi r_{matte}^2\right)}{A_{flat\_matte}}\right)}{\left(1+\frac{\delta(f)}{r_{matte}}+\frac{\delta^2(f)}{2r_{matte}^2}\right)}\right)$$

5. Determine the average $K_{SR\_drum}(f)$ and $K_{SR\_matte}(f)$:

$$K_{SR\_avg}(f) = \frac{K_{SR\_drum}(f) + K_{SR\_matte}(f)}{2}$$

6. Apply Equation 8 to determine total insertion loss of the PCB trace.

$$IL_{rough}(f) = K_{SR\_avg}(f)\left(IL_{smooth}(f)\right) + IL_{diel}(f)$$

Summary and Results

The results are plotted in Figure 10. The left plot compares the simulated vs measured insertion loss for data sheet values and design parameters. Also plotted is the total smooth insertion loss (crosses) which is the sum of conductor loss (circles) and dielectric loss (squares). Remarkably there is excellent agreement up to about 30 GHz by just using algebraic equations and published data sheet values for Dk, Df and roughness.

The plot shown on the right is the simulated (blue) vs measured (red) effective dielectric constant (Dkeff), and is determined by the equations shown. As can be seen, the measured curve has a slightly higher Dkeff (3.76 vs 3.63 @ 10 GHz) than published. According to [6], the small increase in the Dk is due to the anisotropy of the material.

When the measured Dkeff (3.76) was used in the model, for core and prepreg, the IL results shown in Figure 11 (left) are even more remarkable up to 50 GHz!

Figure 12 is a Comparison of the Cannonball model against the H&J model. The results show that the H&J is only accurate up to approximately 15 GHz compared to the Cannonball model's accuracy to 50 GHz.

Conclusions

Using the concept of cubic close-packing of equal spheres to model copper roughness, a practical method to accurately calculate sphere size and tile area was formulated for use in the Huray model. By using published roughness parameters and dielectric properties from manufacturers' data sheets alone, it has been demonstrated that the need for further SEM analysis or experimental curve fitting, may no longer be required for preliminary design and analysis.

When measurements from CMP-28 modeling platform, fabricated with FR408HR and RT foil, was compared to this method, there was excellent correlation up to 50 GHz compared to the H&J model accuracy to 15 GHz.

The Cannonball model looks promising for a practical alternative to building a test board and extracting fitting parameters from measured results to predict insertion loss due to surface roughness.

Supplemental Information

Figure 13 are examples of close-packing of equal sphere models, and their respective equations. The model on the left is the hex-

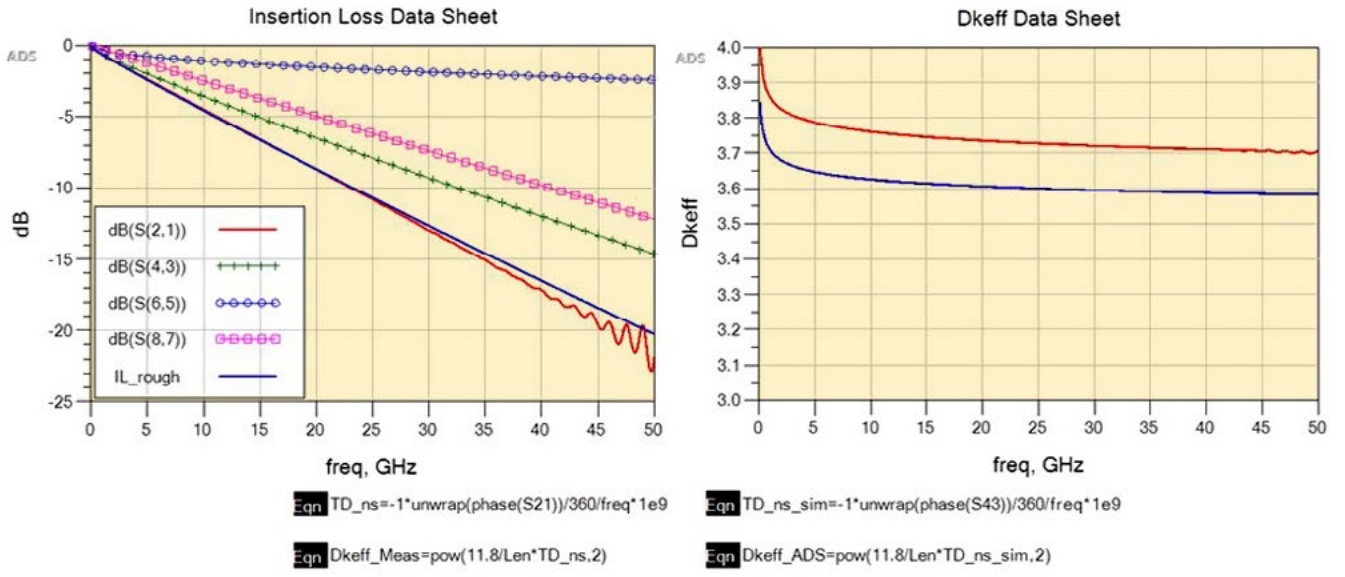


Figure 10: IL (left) for a 6-inch trace in FR408HR RTF using supplier data sheet values for Dk, Df and Rz. Effective Dk is shown right.

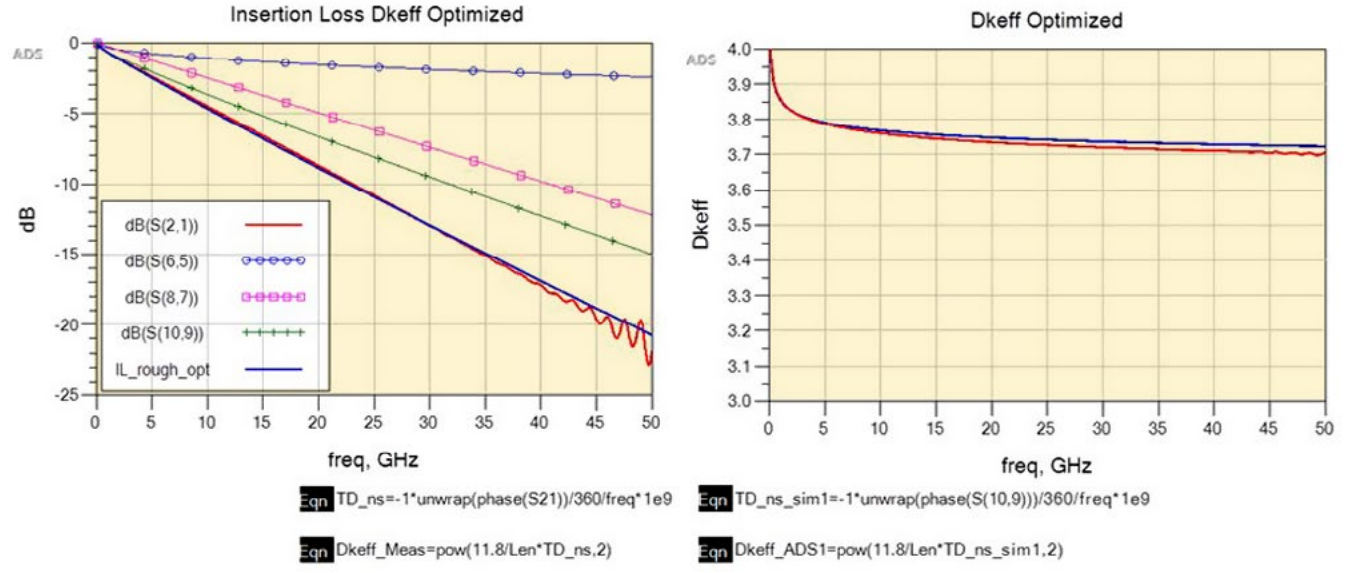


Figure 11: IL (left) for a 6-inch trace in FR408HR RTF and effective Dk (right).

agonal close-packing of equal sphere (HCPES) model [1]; the center is the square close-packing of equal sphere (SCPES) model, or Cannonball model described in this paper; and the right hand figure is triangular close-packing of equal sphere (TCPES) model. All three models give equal correction factor results as shown in Figure 14. **PCBDESIGN**

References

[1] Simonovich, Bert, "Practical Method for Modeling Conductor Surface Roughness Using Close Packing of Equal Spheres," DesignCon 2015 Proceedings, Santa Clara, California, 2015.

[2] Hammerstad, E. Jensen, O., "Accurate Models for Microstrip Computer-Aided Design," Microwave symposium Digest, 1980 IEEE MTT-S

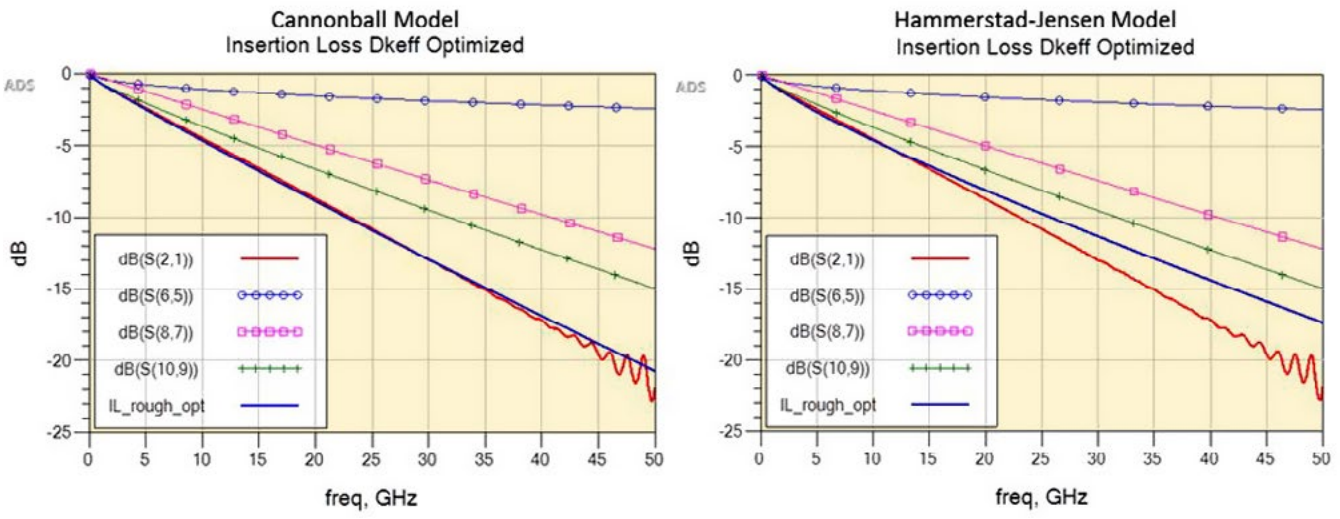


Figure 12: Cannonball model (left) vs Hammerstad-Jensen model (right).

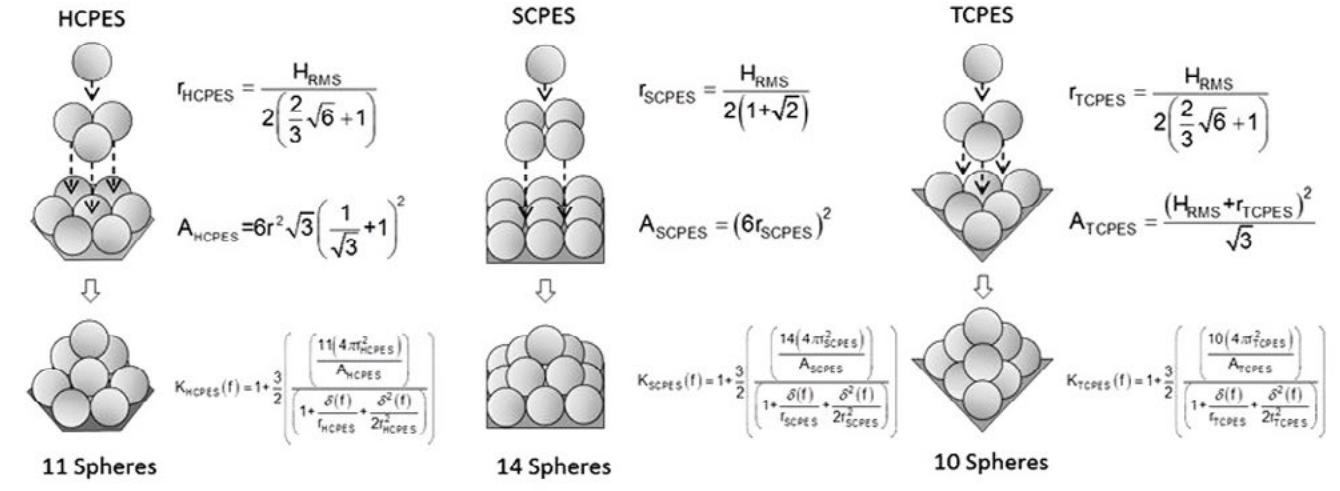


Figure 13: Close-packing of equal sphere model variations. Hexagonal close-packing of equal spheres, HCPES (left) as described in DesignCon 2015 paper [1]; Square close-packing of equal spheres, SCPES (center); and triangular close-packing of equal spheres, TCPES (right).

International , vol., no., pp.407,409, 28-30 May 1980 doi: 10.1109/MWSYM.1980.1124303.

[3] S. Hall, H. Heck, "Advanced Signal Integrity for High-Speed Digital Design," John Wiley & Sons.

[4] Huray, P. G. (2009) "The Foundations of Signal Integrity," John Wiley & Sons.

[5] Y. Shlepnev, "PCB and package design up to 50 GHz: Identifying dielectric and conductor roughness models," The PCB Design Magazine, February 2014, p. 12-28.

[6] Y. Shlepnev, "Sink or swim at 28 Gbps," The PCB Design Magazine, October 2014, p. 12–23.

[7] E. Bogatin, D. DeGroot , P. G. Huray, Y. Shlepnev , "Which one is better? Comparing Options to Describe Frequency Dependent Losses," DesignCon2013 Proceedings, Santa Clara, CA, 2013.

[8] Wikipedia, "Close-packing of equal spheres."

[9] Simberian Inc., Las Vegas, Nevada.

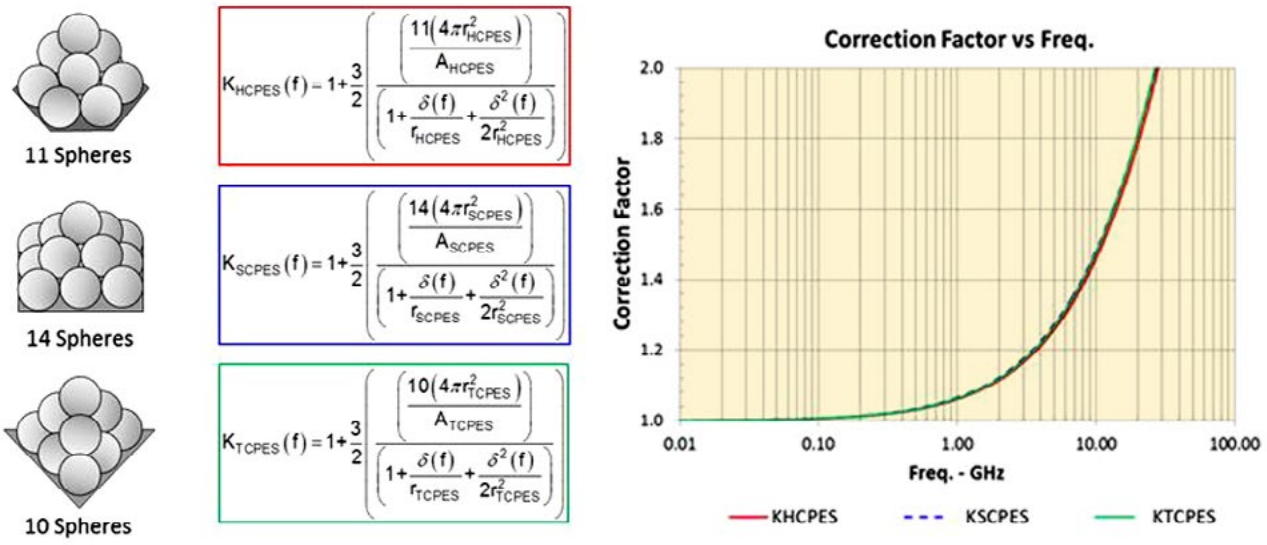


Figure 14: Comparing correction factors for each model. As can be seen all three models provides equivalent correction factors.

[10] Isola Group, Chandler, Arizona

[11] Oak-Mitsui, Hoosick Falls, New York.

[12] Electrochemicals Inc. CO-BRA BOND.

[13] Macdermid Inc., Multibond.

[14] Keysight Technologies EEsof EDA Advanced Design System 2015.01 software.

[15] Wild River Technology, Beaverton, Oregon.

[16] Simonovich, Bert, "Practical Method for Modeling Conductor Surface Roughness Using The Cannonball Stack Principle," white paper, Issue 1.0, April 8, 2015.

Bert Simonovich had a 32-year career at Bell Northern Research/Nortel, in Ottawa, Canada, helping to pioneer several advanced technology solutions into products. He has held a variety of engineering, research and development positions, eventually specializing in high-speed signal integrity and backplane architectures. Simonovich can be contacted through Lamsimenterprises.com.

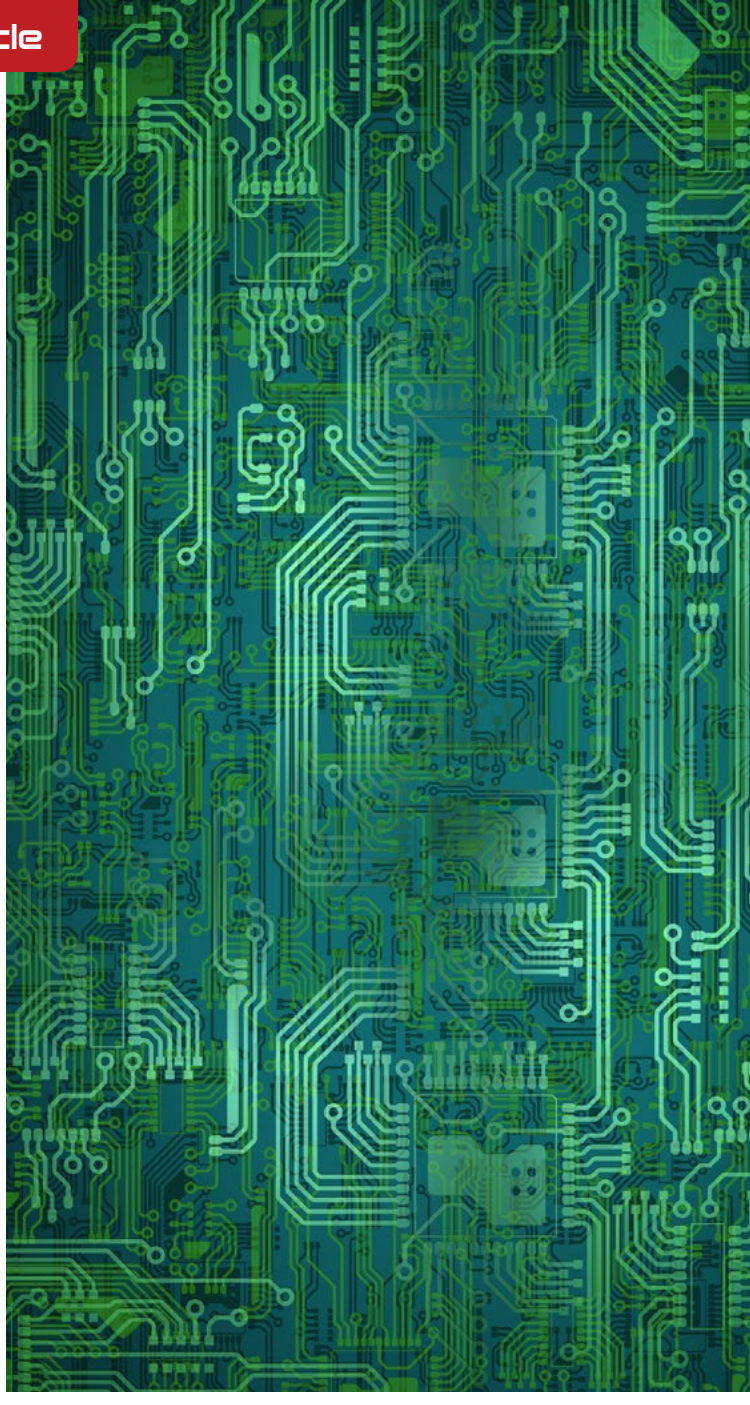
Sodium-ion Hybrid Capacitor as Next-generation Battery

Li-ion (lithium-ion) batteries, which power most portable electronics today, include elements such as lithium and cobalt. As a potential alternative, Na-ion (sodium-ion) batteries have attracted attention because of the abundance and low cost of uniformly-distributed sodium.

However, in order to realize a sodium-ion battery, a pair of compounds capable of intercalation (absorbing and releasing) of sodium ions is required for each of the negative and positive electrodes.

Professor Atsuo Yamada and Associate Professor Masashi Okubo of the University of Tokyo's Department of Chemical System Engineering, in collaboration with the research group of Professor Isamu Moriguchi at Nagasaki University, has clarified that a nanosheet compound comprising titanium and carbon is capable of sodium-ion intercalation.

The Composite Properties of Rigid vs. Multilayer PCBs



by Chet Guiles
ARLON ELECTRONIC MATERIALS

Abstract

Most materials systems used in PWBs (aka PCBs) are composites of resins, fabric substrates and metal cladding. Each of these components has its own unique electrical and mechanical properties that contribute to the final characteristics of the finished laminates, prepregs and fabricated multilayer boards (MLBs). In most cases variables such as glass style and resin content have offsetting impacts on physical vs. electrical properties.

Data sheets often provide data in standard IPC formats, which may look at properties in rigid laminates (nominal 0.062" made using heavyweight glass at 32–40% resin content) rather than thin lams and prepregs used for multilayer PWBs (which more typically average 55% resin content or more). To further complicate the situation, some product lines are manufactured with consistent resin content for all product thicknesses, thus maintaining the dielectric properties while letting the mechanical properties be dictated by the constructions and resin content.

An understanding of what such variations in properties mean and how they relate to what the users will actually encounter is essential to design, manufacturability, assembly and end-use viability. In this presentation we will look specifically at the effect of glass style and resin content on dielectric constant and CTE and discuss how even at the product design level it is important for design engineers to take these into consideration.

Conclusions

In most cases, no single value of dielectric constant or in-plane CTE (representative lami-

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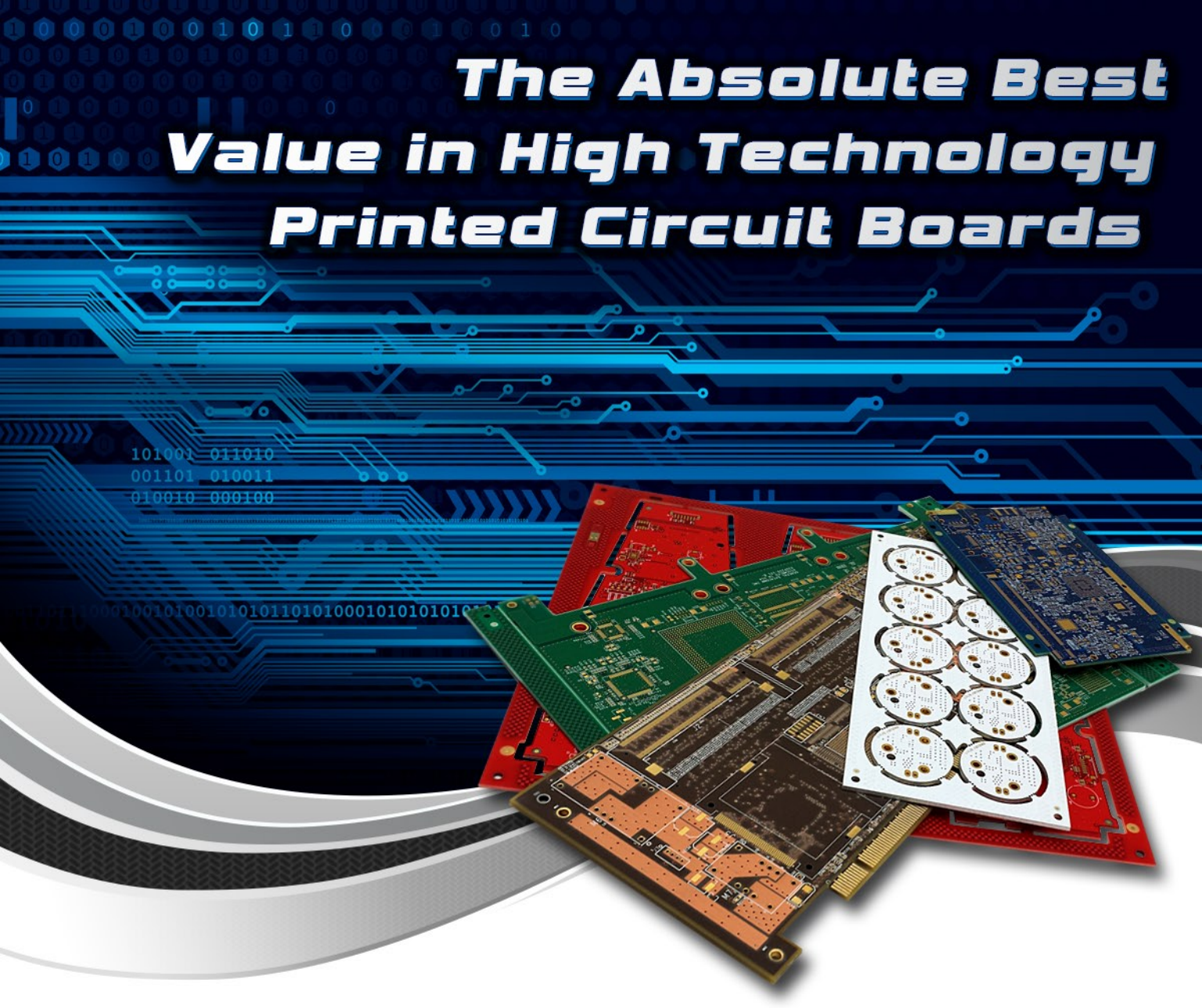

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nate properties that are impacted by resin content variation—obviously there are others as well, but for purposes of keeping this work manageable, we will focus on these two) will hold for all thicknesses of laminate or build-ups for MLBs. In those cases where either or both are critical, it is necessary to control resin content in both laminate and prepreg to ensure that the finished properties fall within the desired and expected ranges.

In some cases, such as with 85N polyimide and 92ML thermally conductive epoxy products, the specific values of Dk and CTE are less critical than other things such as processibility and design flexibility (as for 85N) or thermal conductivity (for 92ML) and so resin contents are allowed to vary so as to meet these needs.

In other cases either CTE (as in 85NT) or dielectric constant (as for Multiclad HF or 25N/FR) are critical needs, and in those cases the resin contents must be held to controlled limits so that the desired properties are consistently held for most or all of the laminate configurations.

Experimental/Assumptions

For purposes of this discussion we will look at three typical resins that are being used in Arlon products: Arlon's 85N pure polyimide resin ("pure" defined here as not containing flame retardant additives that might reduce overall thermal stability) used for high temperature and PTH reliability, 92ML thermally conductive "green" epoxy resin used in boards requiring thermal management, and ceramic-filled MCHF resin (for MultiClad HF) designed for use in high frequency applications.

Additionally, we will consider standard E-Glass (electronics grade woven fiberglass) fabrics as well as nonwoven aramid (NWA) fabric as typical substrates for PWB applications. E-Glass is relatively inexpensive and has been the mainstay of the PWB industry for many years, while nonwoven aramid offers advantages in weight, registration stability and finished product thermal cycling life.

Most properties of a composite such as a prepreg or laminate are based on the volume ratios of the individual components, using formulas that have been refined empirically over many years. Dielectric constant, for example, is proportional to the volume ratios of the resin and glass components adjusted by a factor to give a Dk value that is accurate for the frequency at which the raw material variables are defined.

CTE is computed using the densities of the raw materials, weighted by their volume percentages and individual CTE values using the Schapery Equation (see below). The results given in this work take into account such modifying factors as the weave of glass fabric (which is partially out-of-plane and hence has an effective modulus lower than the theoretical fiber modulus) and the effectiveness of any filler in modifying the modulus of the material. A table of material "effective" properties (working assumptions established based on properties of actual control laminates) for the materials discussed in this paper is included below.

I. Materials Set

- Arlon 85N is based on pure polyimide resin (no added flame retardant or filler).
- Arlon 92ML is a halogen-free high performance (lead-free) epoxy based system containing high loading of thermally conductive ceramic fillers.
- Arlon MCHF (MultiClad® HF Resin) is a second generation multilayerable microwave/RF system containing ceramic fillers consistent with desired electrical and mechanical properties.
- PTFE (polytetrafluoroethylene) with and without ceramic filler is widely used in microwave/RF laminates.
- Arlon 25FR is a first generation ceramic-filled multilayerable microwave system used here for reference, being a system whose build-ups are all held to a constant resin percentage resulting in the same Dk (dielectric constant) and df (dissipation factor, aka loss tangent) for all laminate thicknesses and MLB buildups.
- E-Glass fabric has been the industry standard for longer than this writer can remember.
- Nonwoven Aramid "paper" reinforcement (NWA) is made up basically of short aramid fibers with an appropriate binder.

A note here regarding fillers and the effect of fillers on material properties is in order. While the effect of fillers in modifying the properties of the basic resin is volume dependent, benefit

of the filler property is exponential with regard to loading. For example 50% of TiO2 (Dk~100) in PTFE resin (Dk~2.09) gives a product with a final Dk of about 10, whereas if the effect were linear it would be expected to be about 50. In addition, with many resin systems copper peel strength falls off substantially with higher filler loadings, and where higher levels are essential, resin chemistry adjustments may have to be made to maintain acceptable peels.

Copper foils used in laminates normally include a variety of finishes and "tooth structures." For material like polyimide, a rougher surface results in improved peel strength, while in many microwave/RF products the lower profile coppers are used to minimize the copper foil effect on transmission line loss. We only touch briefly on the impact of copper on physical properties in this paper, but will not try to look at the electrical impact. Where applicable, the assumptions made in this paper assume standard electrodeposited copper foil.

II. Calculating the Composite Properties

The following table of properties shows the effective values of key computational values for the resins and reinforcements covered in this paper. These effective values have been derived based on actual test results for both thin and rigid laminates, and represent a best estimate of how they behave in making a variety of laminate products.

The calculation of dielectric constant from the data shown is done using a standard formula based on the volume ratios of each of the components. For this purpose we have used a composite dielectric constant value for the filled resin systems.

The calculation of CTE values from the data uses the Schapery Equation, which relates composite CTE to weighted values of CTE, modulus and volume.

Schapery Equation:

$$CTE = CTE = \Sigma(a_1v_1m_1+a_2v_2m_2+...a_nv_nm_n) / (\Sigma (v_1m_1+v_2m_2+...v_nm_n)$$

Where:

a = component effective linear coefficient of thermal expansion in ppm/oC
v = volume of each component
m = effective modulus of elasticity (Young's Modulus in mpsi)
n = the number of components making up the composite (resin/reinforcement systems are binary but composites such as PWBs may have multiple layers that contribute individually)

For each resin reinforcement system, we calculated the CTE and the dielectric constant for a range of resin content values that can be related roughly to the typical resin content used

Critical Properties of Materials' Effective Values					
Fabrics		Dk	g/cc Density	ppm/oC CTE	mpsi Modulus
E-Glass		6.4	2.54	6.5	11
Nonwoven Aramid		4.2	1.44	2.5	9
Resin System					
85N Polyimide		3.3	1.3	60	1
PTFE		2.09	2.54	200	0.25
Multiclad®HF		3.35	1.7	30	1.1
92ML Thermal		5.2	2.15	30	1.1
25FR		2.8	1.73	40	1.1

Figure 1: Chart showing critical properties of various materials' effective values.

in various prepreg styles. Typical resin content ranges are as follows

For 85N polyimide on E-Glass
Style 106 68–72%, Style 1080 55–65%
Style 2313 50–55%, Style 2116 50%,
Style 7628 35–40%

For 92ML on E-Glass
Style 104 90%, Style 106 90%,
Style 1080 84%

For Multiclad®HF on E-Glass
Style 104 88–90%, Style 106 86–89%,
Style 1080 80–83%
Style 2313 78%, Style 2116 78%

For 85NT on Nonwoven Aramid
(for constant CTE values regardless of buildup)
All styles 49%

For 25FR on E-Glass
(for constant Dk values regardless of buildup)
All styles 73%

One final note: Dielectric constant values for 85N, 85NT and 92ML are given at 1 MHz, while Multiclad HF is given at 10 GHz. The values for frequencies greater than 1 MHz can be estimated based on the 1 MHz value using a mathematical model. Actual test results (see graph, below) conform well to the model and indicates that for most materials, dielectric constant shifts lower with increasing frequency. The basic math looks like this:

$$Dk@f_i \sim [Dk_o] * [[Dk_i/Dk_o]^{-2(df_o)/\pi}]$$

Where Dk_o = dielectric constant at frequency f_o
Dk_i = dielectric constant at frequency f_i
df_o = loss tangent at f_o

If Dk =3.6 at 1 MHz with df = 0.014, then
Dk at 1 GHz = $3.6*[10^9/10^6]^{((-2*0.014)/\pi)}$ = 3.385

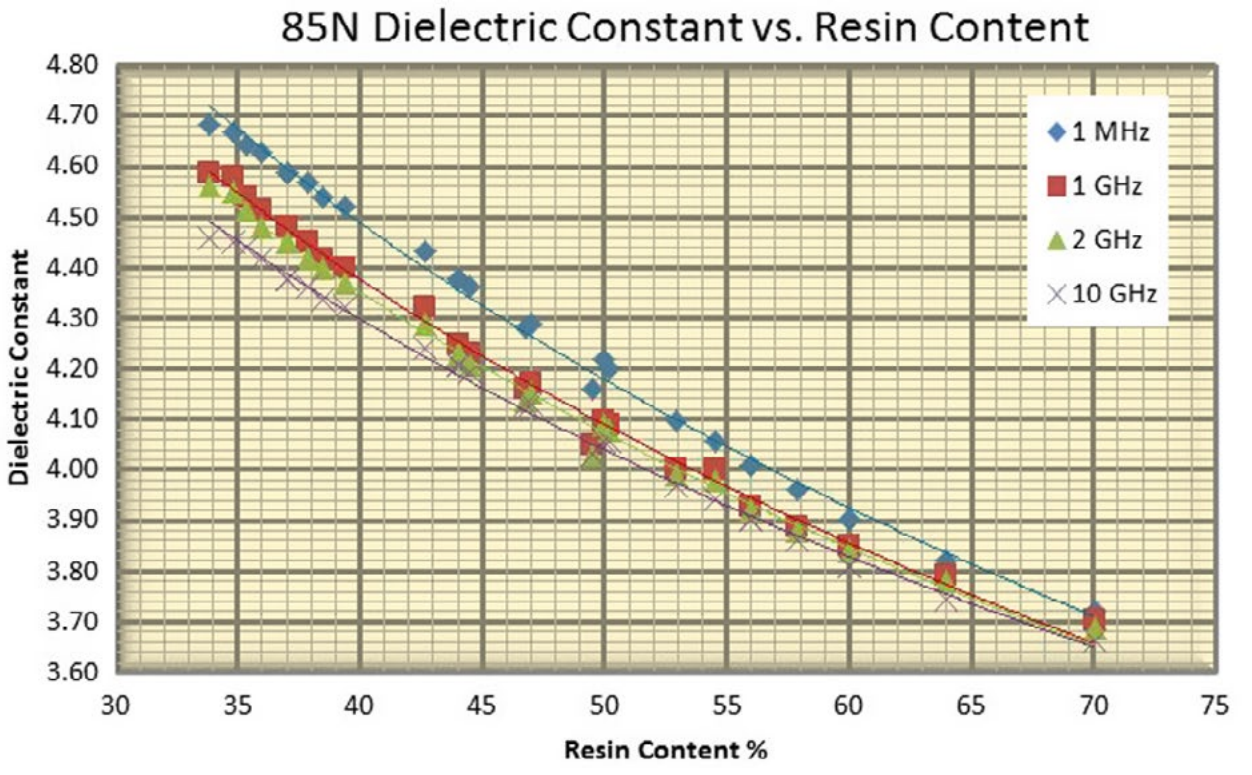

Figure 2.

2015 Programs

May 13–14
IPC Technical Education
Fort Worth, TX, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 9
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Fort Lee, NJ, USA

June 9–10
IPC Technical Education
Chicago, IL, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 10
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Des Plaines, IL, USA

June 12
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Milpitas, CA, USA (San Jose area)

September 27–October 1
IPC Fall Standards Development Committee Meetings
Rosemont, IL, USA
Co-located with SMTA International

September 28
IPC EMS Management Meeting
Rosemont, IL, USA

October 13
IPC Conference on Government Regulation
Essen, Germany
Discussion with international experts on regulatory issues

October 13–15
IPC Europe Forum: Innovation for Reliability
Essen, Germany
Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27
IPC Technical Education
Minneapolis, MN, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

October 28–29
IPC Flexible Circuits-HDI Conference
Minneapolis, MN, USA
Presentations will address Flex and HDI challenges in methodology, materials, and technology.

November 2–6
IPC EMS Program Management Training and Certification
Chicago, IL, USA

November 4
PCB Carolina 2015
Raleigh, NC, USA

December 2–3
IPC Technical Education
Raleigh, NC, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

December 2–4
International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)
Shenzhen, China

Questions? Contact IPC registration staff at registration@ipc.org or +1 847-597-2861

III. Calculated Data

1. Polyimide (85N resin/E-Glass reinforcement) at 1 MHz (Figure 3 and 4).

2. Thermally conductive epoxy (92ML resin / E-Glass reinforcement) at 1 MHz (Figure 5 and 6).

3. Multiclad HF (MultiClad resin / E-Glass reinforcement) at 10 GHz (Figure 7 and 8).

In order to maintain the specification tolerance of dielectric constant around the nominal 3.7, the resin weight percentage needs to be controlled to approximately 80%+/- 0.75%. While this will vary slightly by glass style, the overall system is designed to produce laminates that fall within dielectric constant tolerance of 3.7 +/- 0.06.

4. Polyimide / Nonwoven Aramid (85N resin / NWA reinforcement) at 1 MHz (Figure 9).

Note that with the nonwoven aramid (NWA) reinforced products, the key to consistent performance is CTE control, therefore the resin content is held at a specification value of 49% for all three basic thicknesses of the NWA reinforcement so that the effective CTE is the same for all laminate thicknesses and PWB builds.

IV. Consequences of Material Choices

With most resin systems, the largest impact of varying resin content is the change in intrinsic properties such as dielectric constant and CTE which are mathematically dependent on the resin content and the physical properties of the material. As a result of modifying resin content, CTE and Dk move in opposite directions. While this is obvious when we look at the data, it is something that many do not understand intuitively. It's important that designers associate the choice of resin content, desired thickness, etc., with the results they will obtain.

In general when the resin content increases, several things occur in consequence:

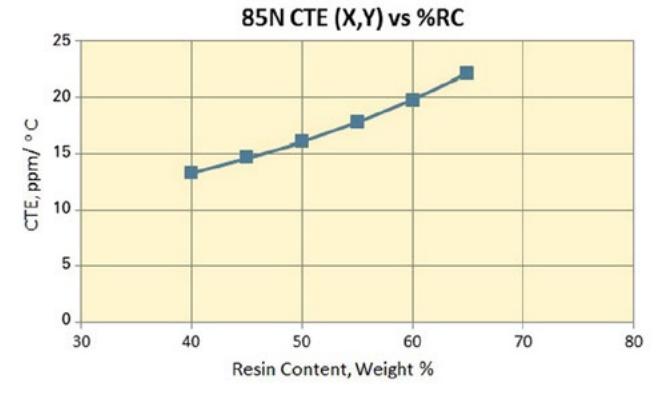

Figure 3.

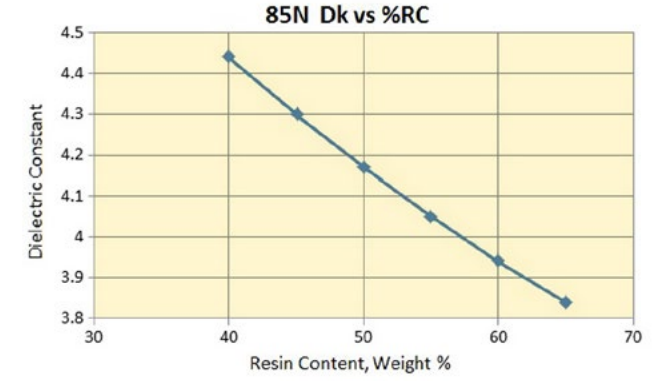

Figure 4.

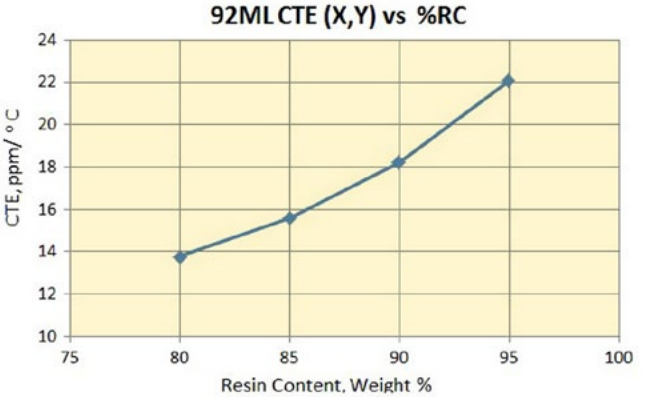

Figure 5.

Figure 6.

1. In-plane coefficient of thermal expansion (CTE) increases because the CTE of the resin (in normal, unfilled systems) is much greater than that of any of the reinforcements we use. Increase in CTE (X,Y) can affect the artwork compensation needed to obtain proper registration; increasing CTE (Z)—perpendicular to the thickness of the board—will impact overall Z-direction expansion, and while this is much harder to calculate theoretically, in general higher Z-expansion will mean more strain (and stress) in plated through-holes, and a decrease in PTH reliability through thermal cycling.

An interesting exception to this is in the case of nonwoven aramid reinforcement, where the Z-direction expansion is inherently greater because of the constraint on X,Y due to the high modulus aramid fibers, and yet the PTH reliability through thermal cycling can be 2–3x better than with the same resin system on a woven glass substrate. The reason for this appears to be that with glass fabrics there are discrete fiber bundles that intersect hole walls and concentrate stresses at those points, which are where most copper barrel cracking failures occur. The more uniform NWA reinforcements do not have the discrete bundles of fibers and as a result, do not tend to isolate or concentrate stresses.

In instances where the value of CTE(X,Y) is important, such as in 85NT nonwoven aramid products where the end-use is for SMT applications requiring a consistent reduced CTE, the resin content of both laminate grades and prepreg sales grades is held to a constant value for all thicknesses of product. This restricts variability in CTE to that caused by normal variability in resin content. The wide range of resin contents experienced with the normal range of glass styles used when using standard E-Glass reinforcement doesn't permit this degree of stability of CTE, or, as we will see, in dielectric constant.

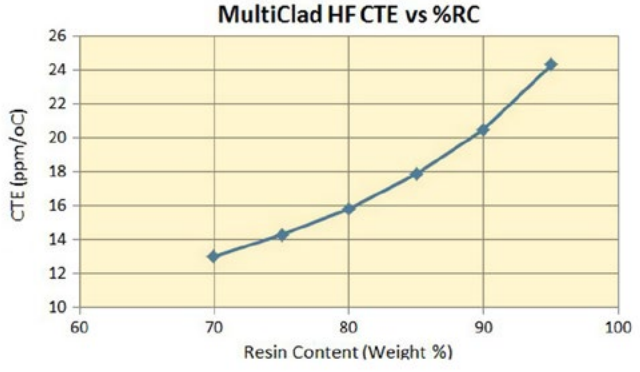

Figure 7.

2. Higher resin contents are inherently more difficult to control and so variability in resin content and flow are more likely in prepregs with higher resin contents. The selection of a higher resin content for any specific glass style then will also affect resin flow and pressed thickness, sometimes in a hard to predict manner that will interact with board design and process variables such as pressure and heat-up rates. Too low a resin content, sometimes desired to control laminated thickness, may result in lack of adequate flow and associated dryness, especially in large areas of relative low pressure

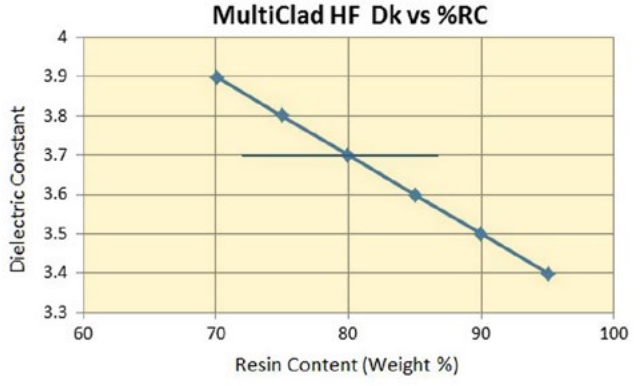

Figure 8.

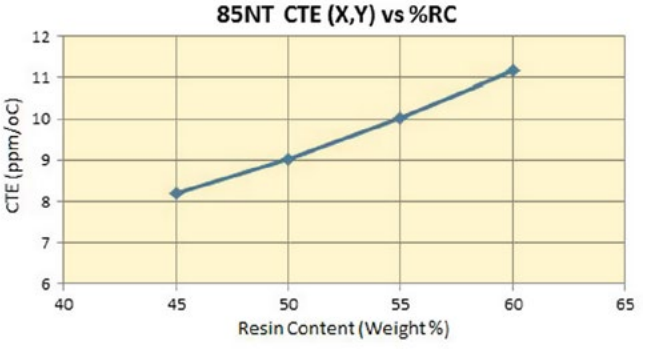

Figure 9.

such as areas where most of the copper is etched away in part of the board, but not uniformly across the panel.

3. As the resin content increases, dielectric constant normally decreases. There may be a few exceptions in the area of very high-dielectric constant systems where the resin has a higher Dk than the substrate, such as in Arlon's Dk 10 products—PTFE/ceramic filled systems—but that's not normally the case. This has an impact on the impedance calculations for any particular design, and if a variety of laminate and prepreg resin contents are used in the various layers of a PWB, some amount of guesswork may be necessary to "design" for a fixed impedance, often 50 ohms for transmission lines.

"As the resin content increases, dielectric constant normally decreases. There may be a few exceptions in the area of very high-dielectric constant systems where the resin has a higher Dk than the substrate, such as in Arlon's Dk 10 products–PTFE/ceramic filled systems–but that's not normally the case."

What this means in practical terms is that in normal systems such as FR-4 and Polyimide made with E-Glass reinforcements, the Dk of each laminate and/or prepreg element will vary depending on the "normal" resin contents for the different styles of glass fabric, typically quite high for thin glass such as 106 (72–75%) and much lower for heavyweight glass used to make rigid laminates such as 7628 (37–42%). As a result data sheets that report properties for rigid laminates (0.023" and above) may show maximum values for dielectric constant that are much higher than those actually obtained in multilayer constructions. A polyimide whose IPC/41 spec calls for a Dk of 5.2 max will actually have a value of 4.0 or less in a high layer count multilayer board using thin laminates and high resin thin prepregs. It's easy to see than in such a case, if impedance is calculated based on the data sheet value, the results may be badly skewed.

To compensate for this, some products such as Arlon's 25N and 25FR, which are primarily designed for use in microwave or RF designs where the principal concern is dielectric constant consistency, are designed such that the resin contents of laminate and prepreg are held to fixed limits such that the specified dielectric constant is held to within the tolerance of resin content manufacturability, as low as +/- 1% or even less. If prepregs or laminates have to be used that do not meet the nominal target resin content, recalculation of Dk may be necessary for layers with active circuitry.

V. PWBs vs. Raw Laminates: The Impact of Copper

Copper foil has a relatively high density and a high modulus of elasticity (Young's Modulus of ~17 mpsi) and a CTE (effective) of roughly 10.7 ppm/°C. (Pure copper CTE is actually about 17 ppm/°C and the 10.7 value reflects performance in actual constructions.) This has a number of impacts on PWB design and function.

1. In plated through-holes (PTHs), copper's expansion coefficient will be less than that of the resin in conventional epoxy or polyimide systems, and so any strain in the hole caused by expansion and contraction of the resin during thermal cycling will impact PTH reliability. This is partly due to "latent defects" caused by large thermal excursions during manufacturing and assembly operations, and partly to the actual amount of Z-direction expansion caused by the CTE of the resin.

For example, copper with a CTE of 17 ppm/°C (in PTHs) will expand 3750 ppm (0.37%) over 210°C range (50°C to 260°C) while epoxy systems will expand as much as 35000 ppm (3.5%) and polyimide systems as much as 16000 ppm

(1.6%) over the same range. Polyimides with high Tg and hence lower overall expansion, will result in lower strain on the copper barrel during thermal expansion and less work hardening due to repetitive expansion/contraction cycles. Laminates with high loadings of ceramic fillers that have reduced Z-direction expansion will also better match the copper and improve PTH reliability.

In the X,Y plane of the board, copper will drive the CTE higher in many instances. Typical epoxy and polyimide boards made with high resin contents will have naturally occurring composite CTEs in the 15–17 ppm/°C range and this will not be a substantial issue. On the other hand, boards made with nonwoven aramid or other materials designed to control CTE for SMT and chip attach applications, need to be designed with as little copper as possible, since copper will drive the CTE of the overall system up in proportion to how much etched copper remains, especially if there are a lot of power/ground planes.

VI. Reading the Data Sheet

Finally, we would offer this advice: "Do not be deceived by the data sheet." This is an old concern of ours, and frequent discussions with customers confirm that it is a widespread issue. Many reported physical properties are based on rigid 0.062" lams (37–40% RC) in accordance with IPC slash sheet requirements.

If your application is for a high-layer count multilayer board and the product does not have a specified value across various resin contents, be sure to ask your supplier what the expected dielectric constant or CTE will be for the range of material you actually plan to use. **PCBDESIGN**

Chet Guiles is a consultant for Arlon Electronic Materials.

Mil/Aero007 Highlights

Zentech's John Vaughan on the Mil/Aero Sector: "It's Headed Up"

I-Connect007 Publisher Barry Matties and Zentech's John Vaughan had a chance to discuss industry concerns within the mil/aero segment at IPC APEX EXPO 2015. The two also shared thoughts on the space industry, and Vaughan detailed Zentech's involvement with National Manufacturing Day, a nationwide effort focused on STEM (Science, Technology, Engineering and Math).

PNC Announces Latest Add-on Qualification to MIL-PRF-31032

PNC is proud to announce the latest add-on qualification of product testing to Military Performance Specification MIL-PRF-31032, CAGE Code 66766. The newest capabilities stem from PNC's continuous improvement of capital equipment.

Exception PCB Earns AS9100 Certification

Exception PCB Solutions Ltd, one of Europe's leading PCB producers, recently secured their AS9100 approval following a recent assessment by BSI (March 2015). AS9100 is the internationally recognised quality management system specialised to the aerospace industry.

FTG Circuits Earns DoD Certification for Flex PCB

Firan Technology Group Corporation announced that its Circuits—Toronto facility has added flexible and rigid-flex printed circuit boards to its qualification under Military Specification MIL-PRF-31032. This certification is in addition to the multiple existing certifications for a wide range of technologies already held by the facility.

Key PCB Makers Strategize to Meet Industry Demands

The computer/peripheral application is expected to witness the highest growth followed by the communication applications. Nippon Mektron, Zhen Ding Technology Holding Limited, Young Poong Electronics Co. Ltd., Unimicron Technology Corp., and Samsung Electro-Mechanics are among the major suppliers of PCBs. The industry players are going for partnership and strategic alliances to deliver unique solutions and to meet the constantly changing industry demands of customers.

Battelle Unveils Breakthrough Anti-Counterfeiting Detection for ICs

"As counterfeiting continues to be a growing issue for both suppliers and manufacturers, ensuring that all components are effectively and accurately verified for authenticity has become an increasingly time consuming and expensive task," said Larry J. House, Cyber Technical Director, of Battelle.

DARPA Programs Simultaneously Test Limits of Technology

Less than one week after releasing Breakthrough Technologies for National Security, DARPA's latest summary of the agency's mission, accomplishments and funding priorities for extending its legacy of technological disruption, the agency today announced four major new programs—evidence of DARPA's commitment to pursuing high-risk/high-reward research and making the impossible possible.

DARPA Shares Vision for the Future

New biennial report describes the agency's mission in the context of today's fast-changing world, and current and upcoming areas of focused investment

Boeing Boosts Imaging, Intelligence Services; Acquires 2d3 Sensing

Boeing has acquired 2d3 Sensing, a wholly owned subsidiary of OMG plc specializing in motion imagery processing of critical intelligence, surveillance and reconnaissance data generated from aerial platforms.

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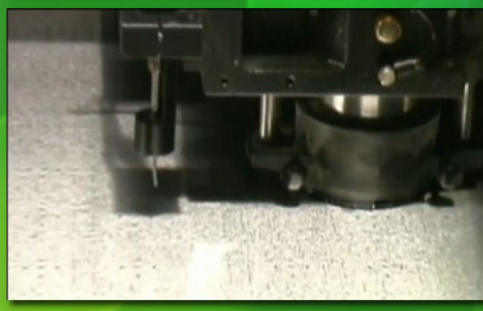

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Electronic Design Training Crucial to Industry Growth

by Bob Sadowski
QUADRA SOLUTIONS

The electronics industry is in a growth period. In 2015, the European electronics industry is set to grow by around 4% over the previous year. The demand for consumer electronics is growing worldwide year-on-year, driven by demand for TVs, headphones and high-definition sound systems. Within commercial and industrial industries, the requirement for smarter, more efficient electronics is also driving strong growth.

In the UK, the electronics industry contributes over £80 billion (approximately US$120 million) to the economy, representing 5.4% of UK GDP, employing over 850,000 people. There is, however, in many countries, a growing concern around labour shortages within the electronics industry, with worries over appropriate workforce skill levels growing.

The story is no different anywhere else, with American small/medium enterprises (SMEs) under similar pressure to recruit and train the most appropriate staff to undertake PCB design work. The U.S. is the world's largest producer of electronic products, accounting for around 21% of the world's total.

A recent study found that 72% of manufacturers believe a labour shortage of electronic design professionals exists, and two-thirds have found difficulty recruiting production and design engineers in the past two years. One of the most adversely hit industries is PCB fabricators, designers and manufacturers, a sector of which 95% are SMEs.

As these companies look to cut costs and drive efficiencies to stay competitive, many larger organisations have considered moving manufacturing functions to other countries to take advantage of cheaper labour costs. This, unfortunately, only further compounds the reported skill shortages within the UK, Europe and U.S.

A recent study by IPC highlights a number of reasons for these concerning issues. Demand for talent in electronics manufacturing has grown faster than the supply, due in part to an ageing workforce. Another IPC study of the North American Electronics industry found that leading issues impacting recruitment included a

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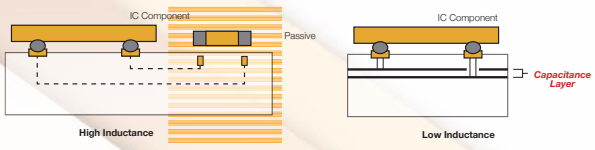

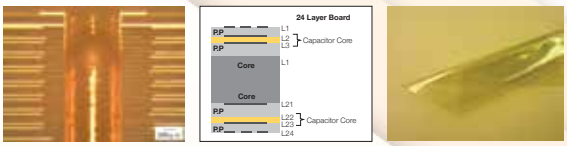

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negative public perception of the industry, job candidate salary and development expectations and continuous professional development opportunities within the industry.

Within the past few years, there has been a greater focus on encouraging young people into manufacturing and electronic industries, with the resurgence of apprenticeships and a greater push for organisations to work in unison with local government, business networks and education providers.

There are many examples of areas where these initiatives have been successful, such as one lead by the UK Electronic Skills Foundation, a great example of where bridging the gap between employer and education providers has helped to promote the industry. Electronics organisations from Cambridge held competitions for students in order to stimulate interest and raise awareness of the electronics industry and its career opportunities. It is hoped that projects like these will gain momentum and be championed elsewhere.

The shifting focus of schools towards engineering and manufacturing subjects has seen a rise in demand for engineering and technology degree courses. However, this does not seem to have had the same effect on applications for electronic engineering degrees. Nor does it seem to have increased the number of people entering apprenticeships within the industry. A recent Young Enterprise survey of 28 UK blue-chip businesses found 75% of managers believed graduates entering the workforce did not possess the skills required.

One of the areas that have been highlighted as a concern for the industry is the lack of opportunities once in electronics-based employment. Many of these careers require a degree and have an entry-level starting salary of £18,000; this figure is £8,000 below the average starting salary for a graduate. It is also perceived that once in an electronics-based career, the opportunities for growth and continuous development are more limited than other industries.

And it's not just the employees that are missing out. This lack of training can have a major impact on businesses. An IDC study showed that without training, employees only use an average of 13% of the features in their software tools. This means that the other 87% of features available within the software are a wasted investment if further training is not undertaken. The study also highlighted that electronics organisations were more likely to gain greater benefits from workforce training due to the rate of change within the industry and the need for staff to be adaptable and update their skills.

“The shifting focus of schools towards engineering and manufacturing subjects has seen a rise in demand for engineering and technology degree courses. However, this does not seem to have had the same effect on applications for electronic engineering degrees. Nor does it seem to have increased the number of people entering apprenticeships within the industry.”

Training can be a crucial to successful development of projects, staff retention and innovation. But the trend seems to be that many companies have dramatically cut training programmes for new employees. In a recent survey of electronic design professionals it was found that they felt there were insufficient opportunities for growth and development and that given the opportunity to undertake further training would be keen to do so.

Continuous development is a critical element for the industry, and IPC is now expanding its training programmes to ensure the skills of the electronics industry are keeping pace with the industry. The Certified Interconnect Designer (CID) qualification seeks to enhance and improve the skills of individuals in the electronics industry and provides delegates with the

foundation of design decision-making, component placement, track routing and assembly issues, all of which need to be met to create high quality and effective end products. More and more companies expect electronic engineers to be trained to this level and the qualification ensures a level of efficiency and effectiveness is maintained during design work.

Qualifications such as this one and the initiatives in schools are a great step in the right direction to providing an environment for the electronics industry to thrive. But employers, employees and the industry need to embrace the changes and challenges or face being left behind. Investment in the future electronics professionals is a key talking point within the industry and even though the subject is much debated and highlighted as crucial to delivering high quality design work, it is still one of the industries least likely to invest in the recruitment, retention and development of staff. **PCBDESIGN**

References

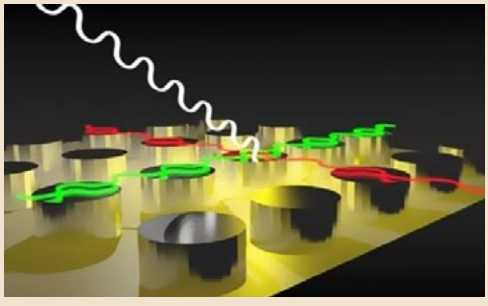
1. IPC 2015 report
2. Newelectronics.co.uk
3. Tech UK
4. USA Today

Bob Sadowski is an applications consultant with Quadra Solutions Ltd, the Zuken reseller for CADSTAR in the UK, Ireland, Benelux, Sweden and Norway.

Putting a New Spin on Plasmonics

Researchers experimentally demonstrated that patterning of magnetic materials into arrays of nanoscale dots can lead to a very strong and highly controllable modification of the polarization of light when the beam reflects from the array. This discovery could increase the sensitivity of optical components for telecommunication and biosensing applications.

The coupling between light and magnetization in ferromagnetic materials arises from quantum mechanical interactions. These interactions result in magneto-optical effects that modify the properties, such as the polarization axis or intensity of the light. Interactions between light and matter are enhanced at the nanoscale. This is a key motivation in the field of plasmonics, which studies light interacting with metal nanostructures.



A nano-sized, metallic nanoparticle behaves very much like an antenna for visible wavelengths; such antennas are familiar to us in numerous everyday devices that operate on much longer radio- and micro-waves. The researchers took advantage of a phenomenon known as surface lattice resonances in which all the nanoparticles radiate in unison in an array. The key to this is to assemble the magnetic nanoantennas on a length scale that matches the wavelength of the incoming light.

In periodic arrays, nanoparticles interact strongly with each other, giving rise to collective oscillations. Such behavior has been reported in noble metal nanoparticles and researched extensively at Aalto University in the Quantum Dynamics research group.

Now, a collaborative effort between QD and the Nanomagnetism and Spintronics (NanoSpin) group shows that such collective oscillations can also be observed in magnetic materials. The surface lattice resonances enhance the light polarization change in ferromagnetic materials, the so-called magneto-optical Kerr effect.

The joint team used the nanofabrication facilities in the Micronova cleanroom as well as the electron microscopy tools available in the Nanomicroscopy Center.

TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Redefines PCB Landscape with New PADS Family

Mentor Graphics has launched three new PADS family products starting at the unprecedented pricing of $5,000 to address the advancing needs of the independent engineer. PADS offerings leverage technologies found in Mentor Graphics' flagship Xpedition product, to tackle the most advanced design complexity challenges.

2 Learn How to Get More than 32 Gb/s from PCBs

The new course is titled "Lee Ritchey: Very High Speed." Slated for May 22 in Stockholm, it covers fast differential pair signal pairs for everything from USB and PCIe to the fastest connections at 32 Gbps and more. Participants can look forward to learning about designing PCBs, how to avoid the pitfalls and also how and how costly HDI techniques can be avoided.

3 Zuken Establishes Local Subsidiary in India

Zuken has established Zuken India Private Limited, a local subsidiary, in Bengaluru (formerly Bangalore, Karnataka State), India. Ramkumar G, the country sales manager of Zuken India, has rich experience in building relationships with advanced technology companies in India. He said, "Zuken India aims to become the most trusted electronic design solution partner in India."

4 Cadence Expands OrCAD PCB Portfolio

Cadence Design Systems has announced five new OrCAD products and three key feature updates as it celebrates 30 years of continued OrCAD design and innovation. The expanded OrCAD portfolio delivers additional high-speed design capabilities that address productivity and time-to-market challenges.

5 Mentor Graphics Restructures Workforce to Focus on Strategic Priorities

Approximately 110 North American Mentor Graphics employees have elected to participate in a voluntary early retirement program. CEO Walden C. Rhines said, "These restructuring activities will enable Mentor to focus personnel and resources on priority opportunities and regions of the world, deliver long-term growth and build shareholder value."

6 EDA Consortium: Record Q4 Industry Revenue, but PCB Drops

The EDA Consortium (EDAC) Market Statistics Service (MSS) has announced that EDA industry revenue increased 11.9% for Q4 2014 to a record $2.1 billion, compared to $1.88 billion in Q4 2013. But PCB/MCM revenue dropped 7.6% from the same year-ago period.

7 Quadra Solutions Named Sole UK Training Provider of IPC CID Courses

Quadra Solutions have this month been named as the sole UK provider of the Certified Interconnect Designer (CID) training course. The qualification, accredited by IPC, is to be delivered by Quadra's highly skilled and experienced trainers at their specialist training facility in Lancashire.

8 Improving PCB Design with Advanced Circuits' PCB Artist

Advanced Circuits' free PCB layout software PCB Artist has become a favorite not only with engineering students but also advanced engineers due to its easy schematic-to-PCB layout, Gerber format, autorouter, and extensive library of over 500,000 parts.

9 EIPC to Hold 2015 Summer Conference in Berlin

EIPC will hold its 2015 Summer Conference in Berlin, Germany, on June 18-19. Speakers include EIPC Chairman Alun Morgan, who will present a market outlook, followed by such luminaries as Dr. Ivan Ndip, Lars Böttcher and Dr. Olaf Wittler, all from Fraunhofer IZM; Walter Huck from IEC; Martyn Gaudion of Polar Instruments; and speakers from AT&S, Thales, Cimulec, Atotech, Taiyo, Camtek, First EIE, Du Pont and Cambridge Nanotherm.

10 Sparton Acquires Hunter Technology Corporation

Sparton Corporation has completed a merger with Hunter Technology Corporation, a provider of PCB design and assembly services, in a $55 million all-cash transaction. "We are looking forward to combining forces with Sparton and taking the next step in the evolution of Hunter Technology," said Joe O'Neil, President of Hunter Technology.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Wisconsin Expo & Tech Forum
May 12, 2015
Milwaukee, Wisconsin, USA

IPC Technical Education
May 13–14, 2015
Fort Worth, TX, USA

International Conference on Soldering & Reliability 2015
May 19–21, 2015
Markham, Ontario, Canada

Toronto SMTA Expo & Tech Forum
May 21, 2015
Markham, Ontario, Canada

Zuken Innovation World 2015 Americas
June 1-3, 2015
San Diego, California, USA

Huntsville Expo & Tech Forum
June 4, 2015
Huntsville, Alabama, USA

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
June 9, 2015
Fort Lee, New Jersey, USA

IPC Technical Education Courses
June 9-10, 2015
Chicago, Illinois, USA

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
June 12, 2015
Milpitas, California, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **RON MEOGROSSI**

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IPC Standards Update

July:
Supply Chain Management